A 10 GHz Frequency-Drift Temperature Compensated LC VCO with Fast-Setting Low-Noise Voltage Regulator in 0.13 um CMOS

Hiroshi Akima, Aleksander Dec, Timothy Merkin, and Ken Suyama

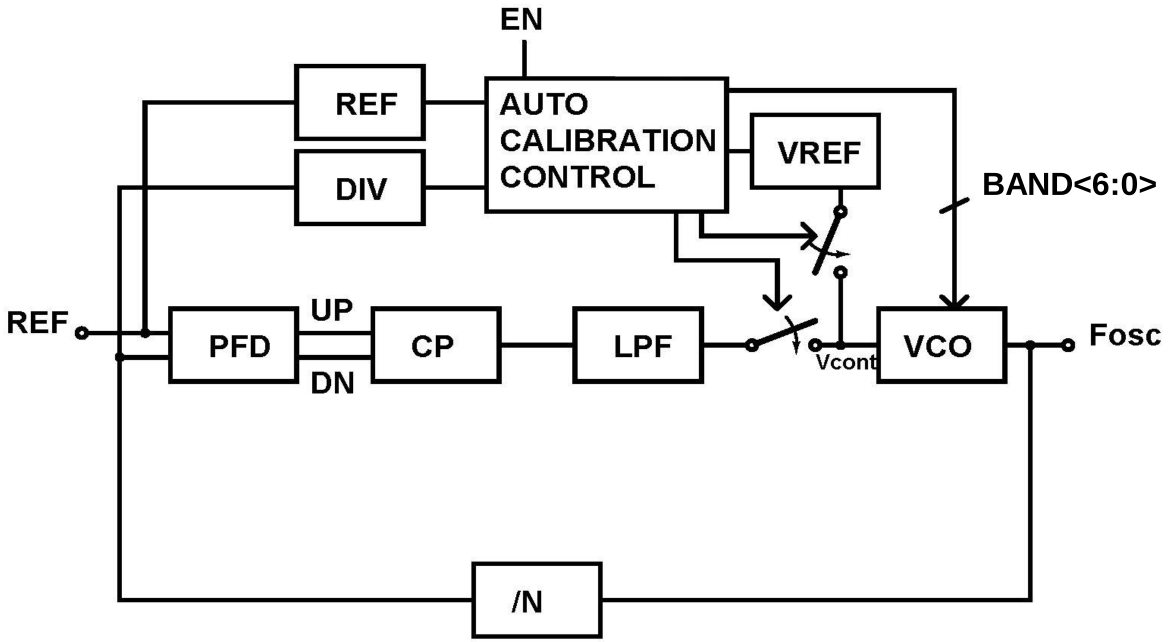
Epoch Microelectronics, Inc., Tarrytown, NY

Motivation

- Requirement for this LC VCO
  - Low frequency-drift over temperature
  - Low VCO supply pushing
  - Minimize noise contributions from bias circuits

- A solution: Integrated temperature compensation circuit

PLL & VCO Tuning

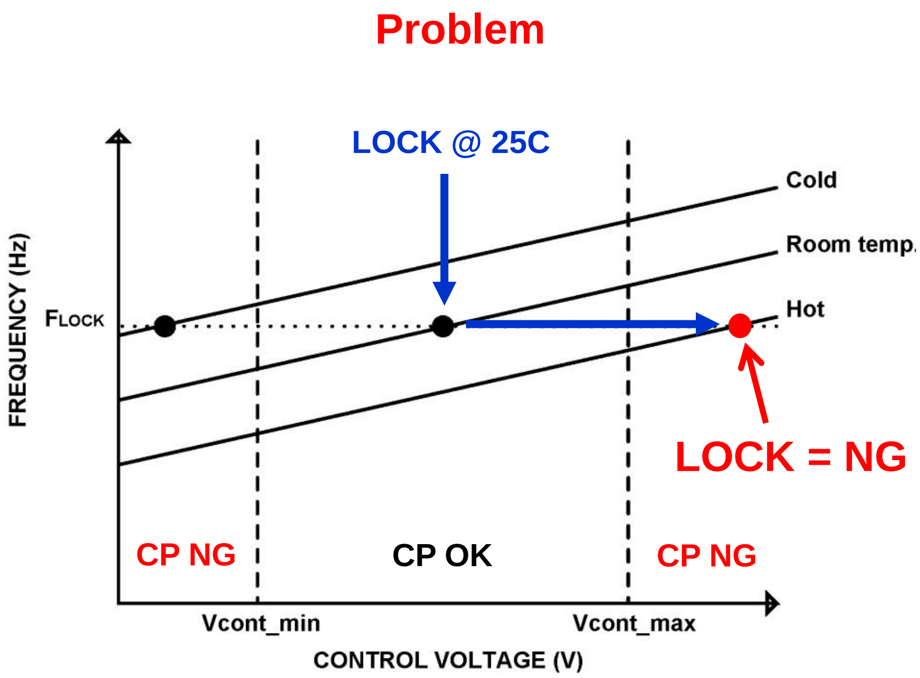


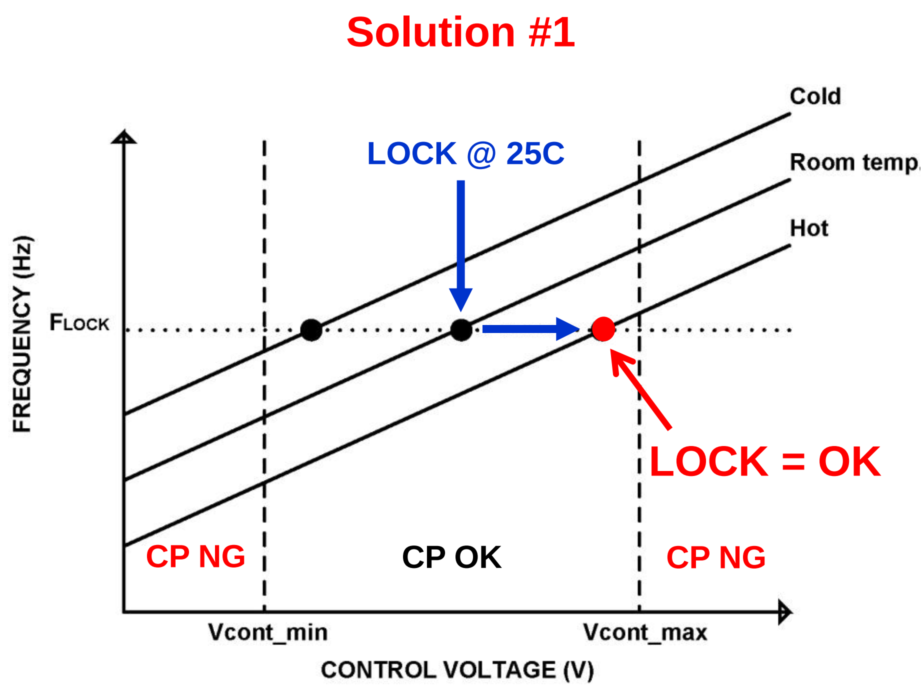
PLL cannot be re-locked after band calibration in continuous operation applications. (Ex. WCDMA / TV)

→A temperature drift of VCO oscillation frequency and supply pushing are critical.

Solution #1: Large VCO Gain

Example: PLL locked @ room temperature and chip gets hot during operation



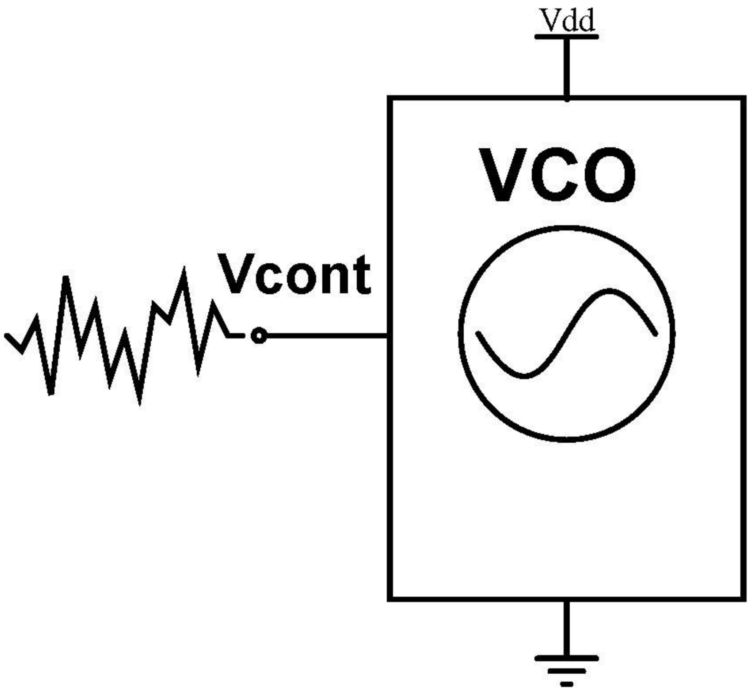


A Large VCO Gain to compensate temperature-drift

Problems:

- High sensitivity to noise coupled onto control line
- Not effective if varactor temperature dependency dominates

FM Noise Contributions



$$K_{VCO} = \frac{\partial fosc}{\partial Vcont}$$

$$L(f_m) = 20\log\left[\frac{2FkT}{P_s}\left(\frac{f_o}{2Q_L f_m}\right)^2\left(1+\frac{f_k}{f_m}\right)+\frac{|K_{VCO}|^2}{2f_m^2}S_{Vcont}\right]$$

Any noise on control voltage contributes VCO phase noise through frequency-modulation.
Therefore, control voltage sensitivity K_{VCO} of the VCO oscillation frequency should be minimized.

FM Noise Contributions (cont'd)

$$L(f_m) = 10\log\left[\frac{2FkT}{P_s}\left(\frac{f_o}{2Q_L f_m}\right)^2\left(1+\frac{f_k}{f_m}\right)+\frac{|K_{VDD}|^2}{2f_m^2}S_{Vcont}\right]$$

$L(f_m)$: phase noise in dBc/Hz

f_o : frequency of oscillation in Hz

f_k : flicker noise corner frequency in Hz

f_m : frequency offset from the carrier in Hz

F : noise factor for the active devices

k : Boltzmann constant in J/K

T : temperature in Kelvin in K

P_s : singal power of the oscillator in W

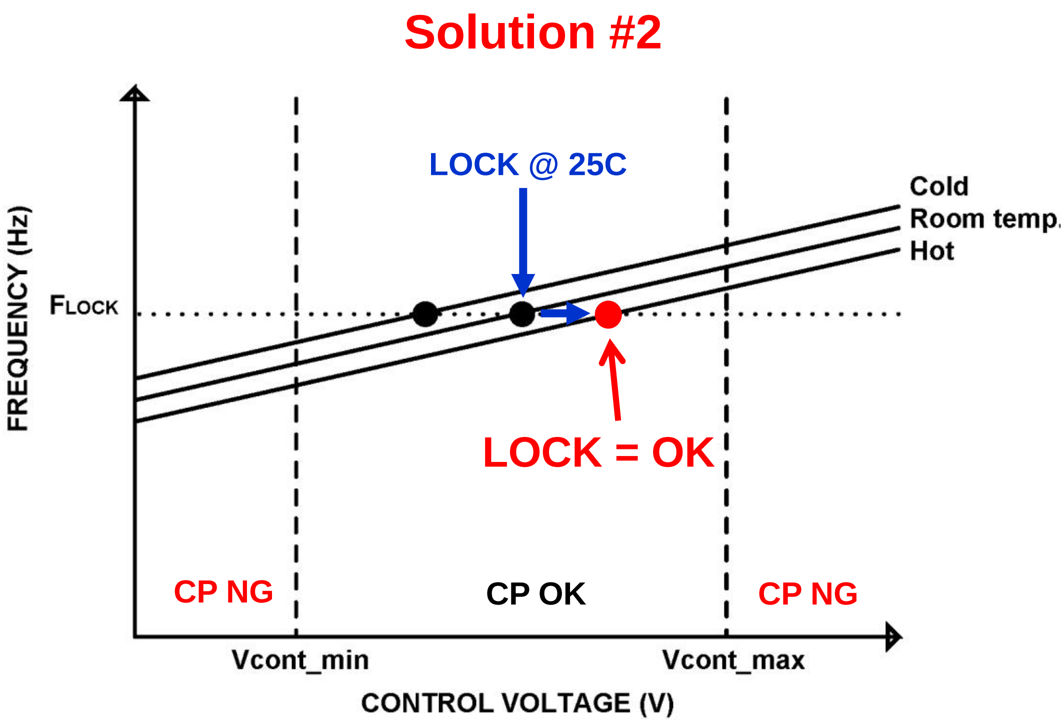
Q_L : loaded quality factor

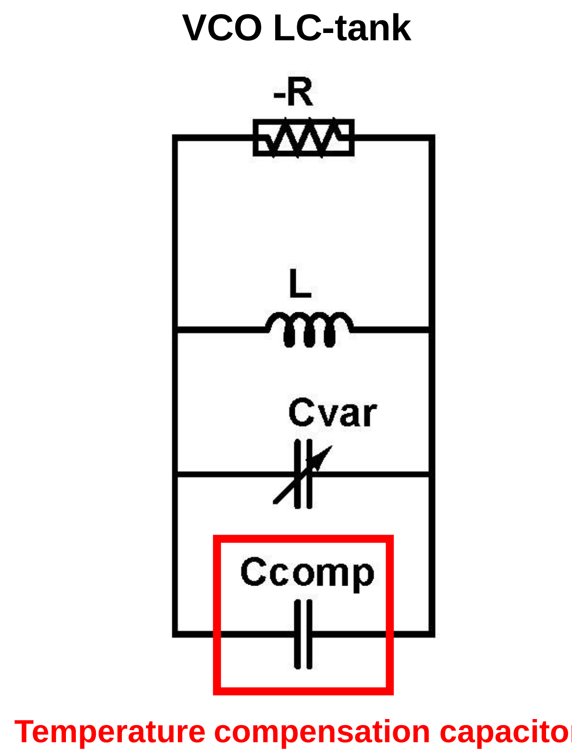
K_{VDD} : sensitivity of the oscillation frequency for the supply voltage in Hz/V

S_{Vcont} : voltage noise spectral density of the control voltage in V^2 / Hz

Reference: A.Aktas, and M. Ismail, CMOS PLLs and VCOs for 4G Wireless, Kluwer Academic Publishers, 2004.

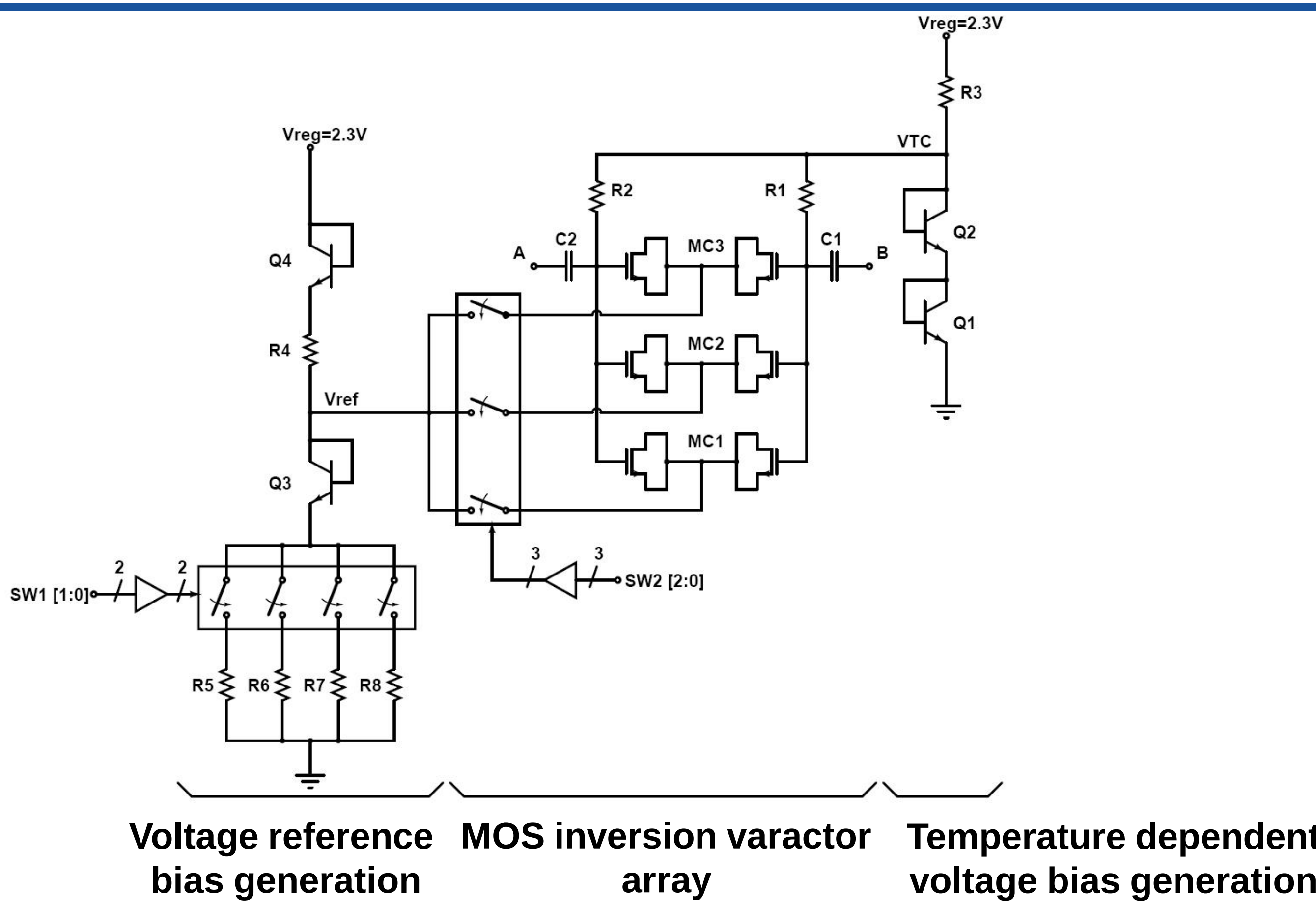
Solution #2: Temperature Compensation





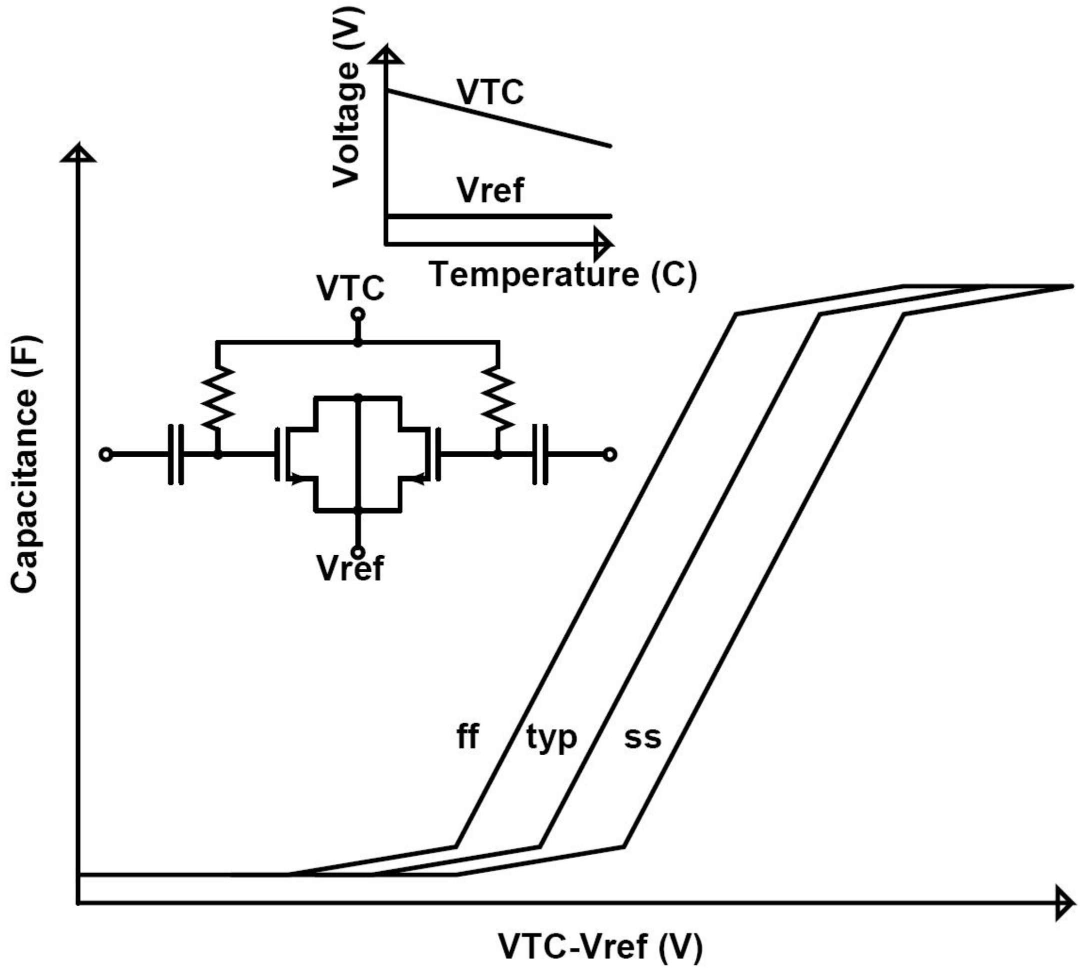
Temperature compensation with low *Kvco* is desirable.
- Increases capacitance at cold
- Decreases capacitance at hot

Temperature Compensation Concept



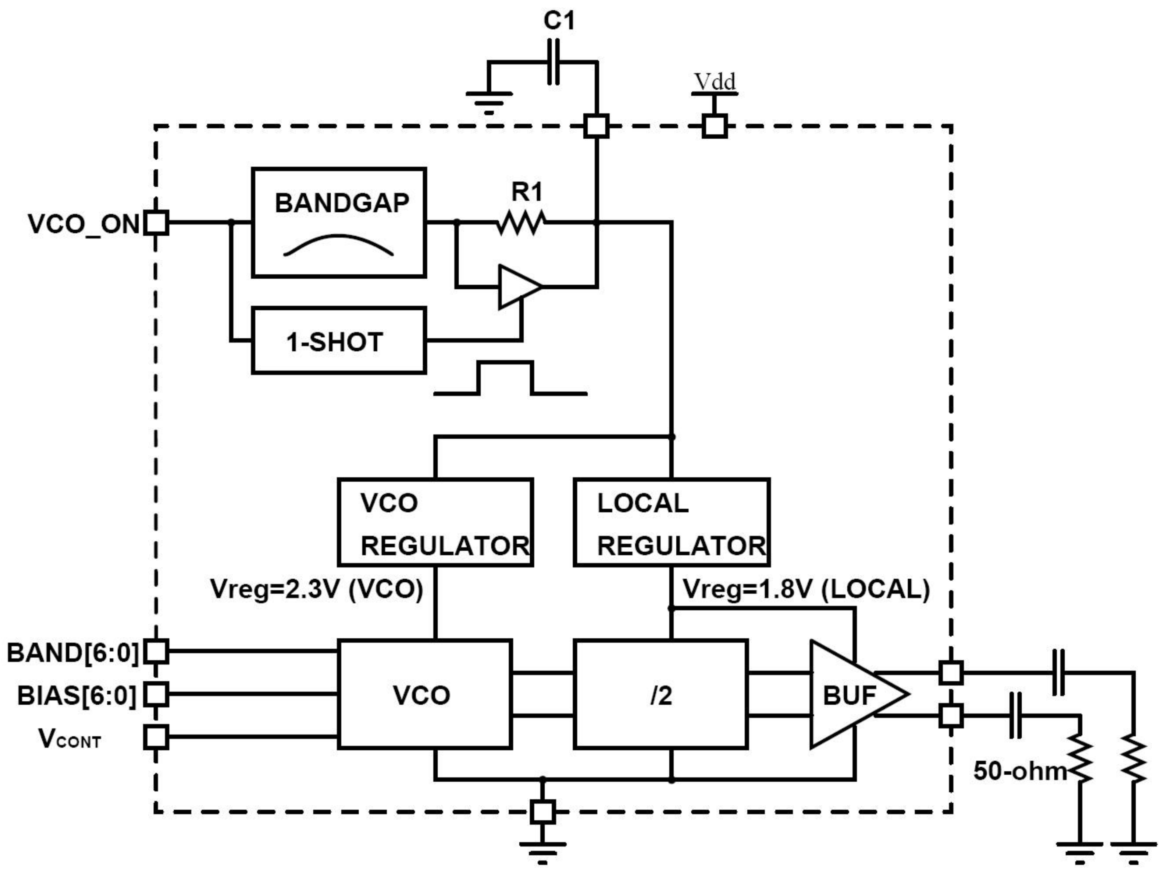
- MOS inversion capacitor based
- Use negative temperature coefficient of BJT's V_{BE}
- Programmable bias and capacitance for simulation and measurement discrepancy, and PVT variations

Compensation Circuit Bias



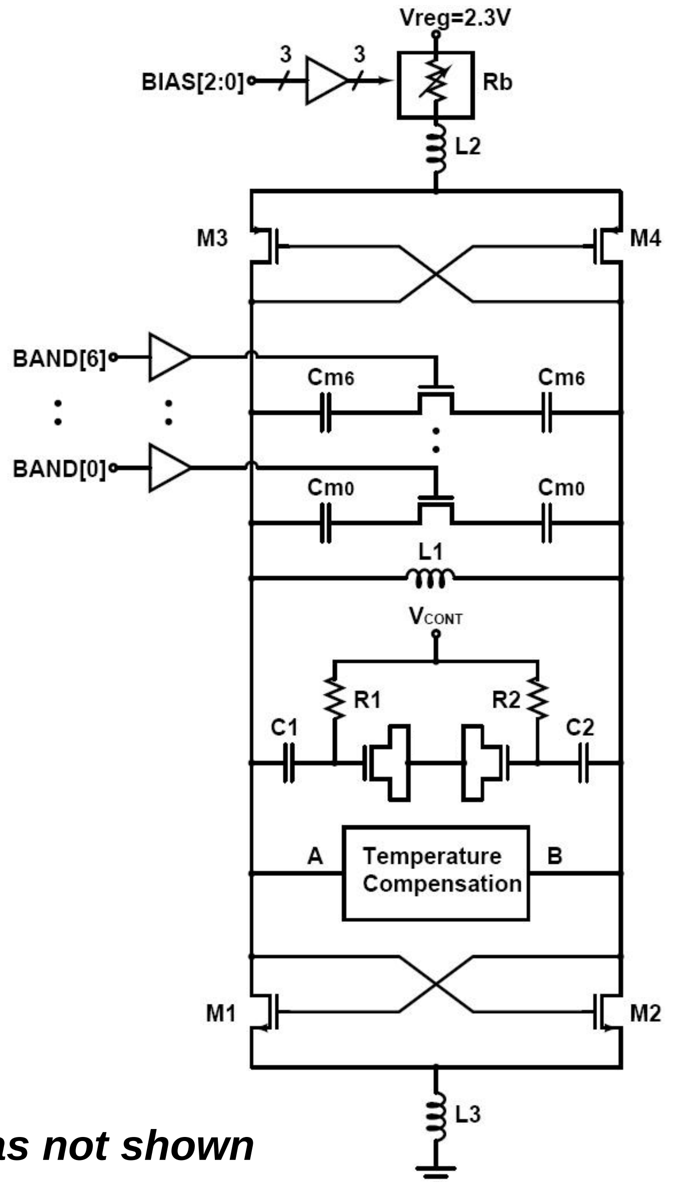
VTC – Vref varies with temperature for compensation.

Test Chip Diagram



- A low noise fast settling regulator for good VCO pushing
- Frequency divider because final application needs 0/90 degree phases
- Output buffer to drive a 50-ohm measurement equipment

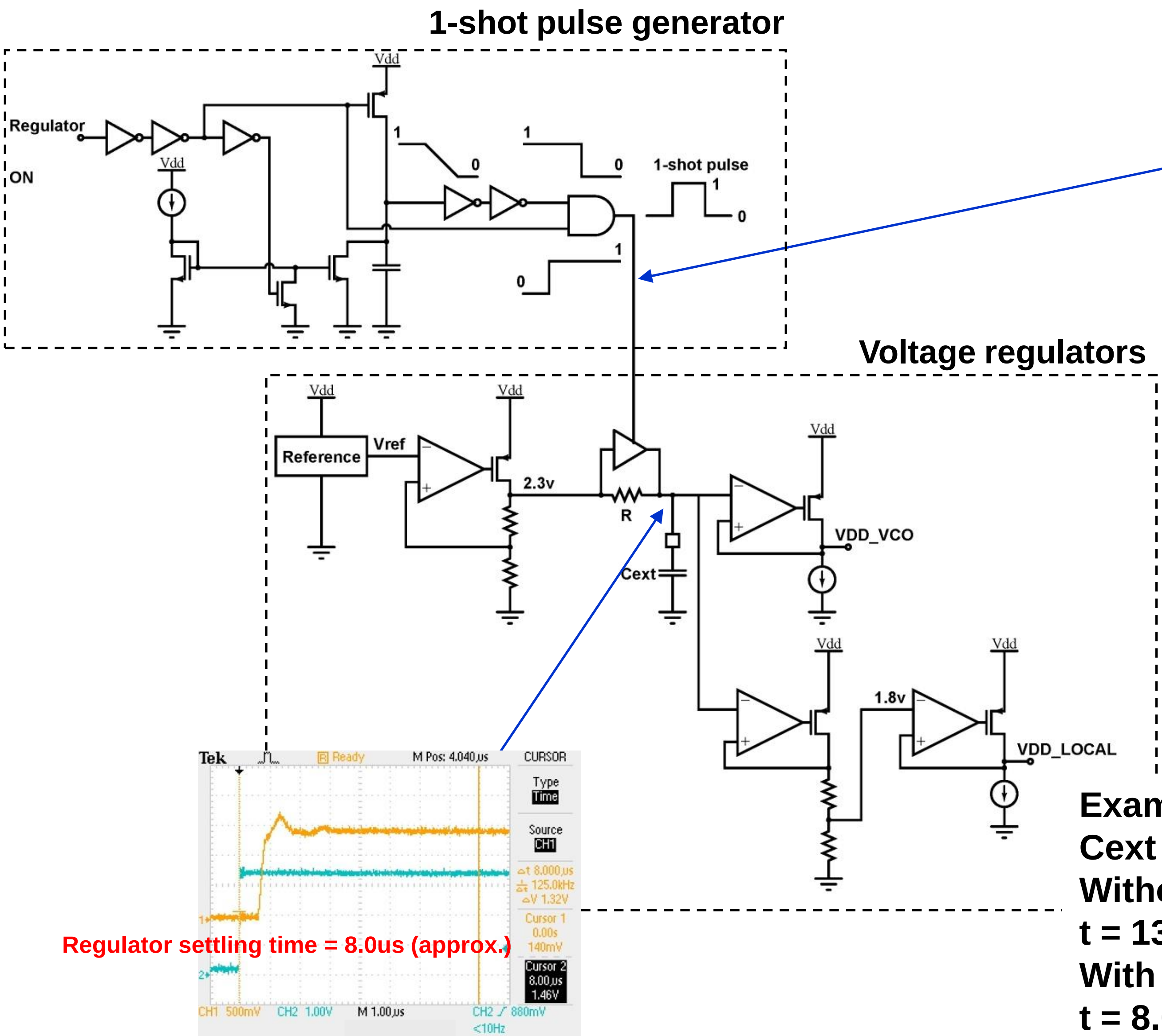
VCO Schematic

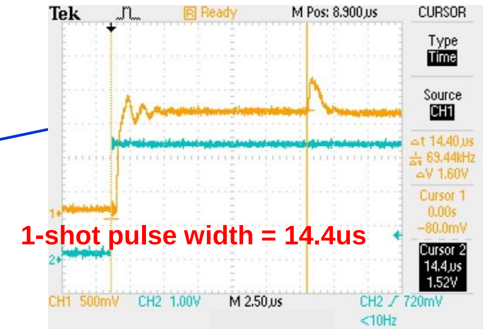


- 7-bit binary weighted MIM capacitor array for large frequency coverage
- MOS inversion varactors for fine frequency tuning
- L2 and L3 for better resonator Q
- VCO bias 3-bit programmable for phase noise optimization at post fabrication process

NOTE: Bias not shown

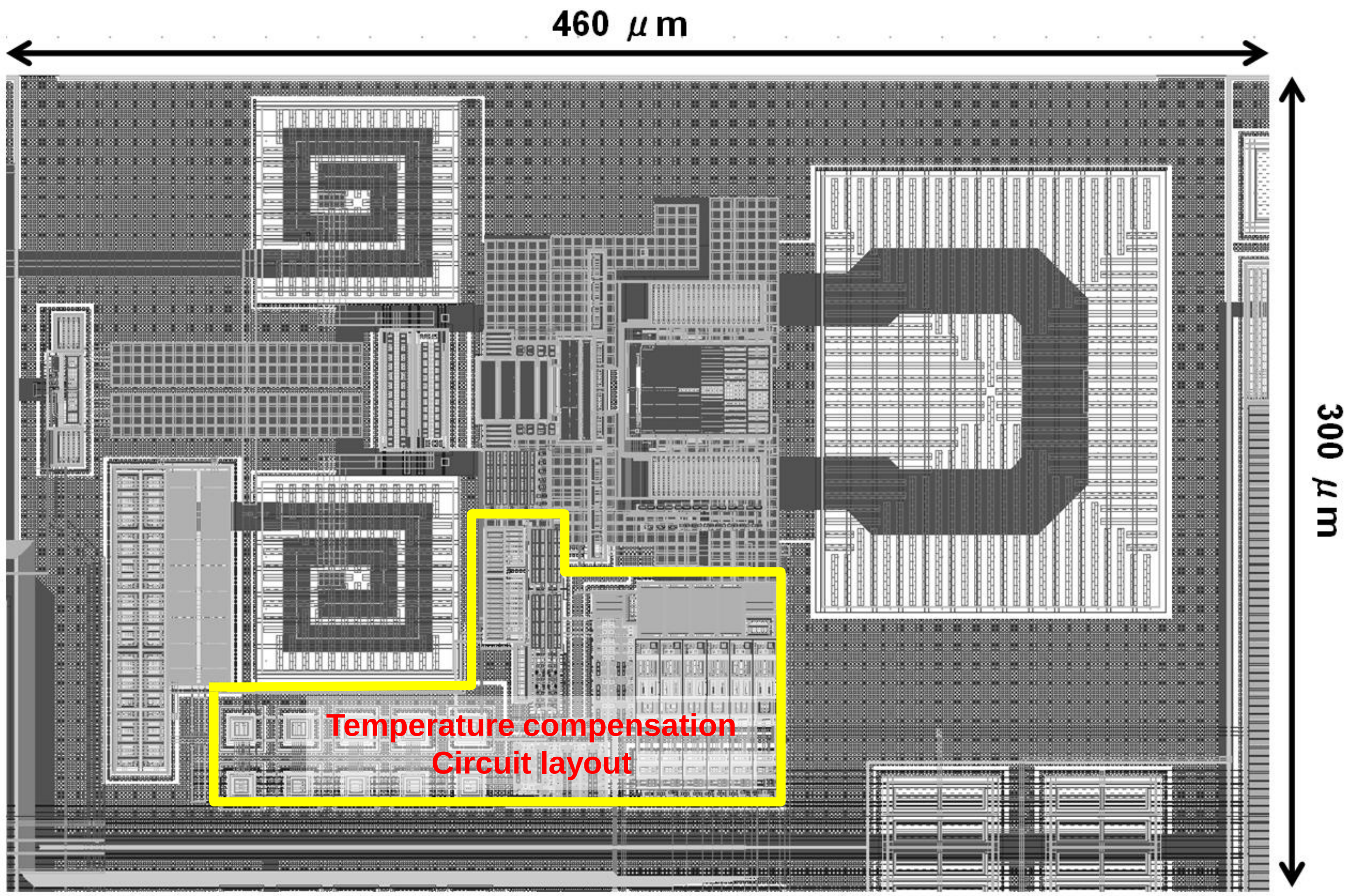
Low Noise Fast Settling Regulator Schematic





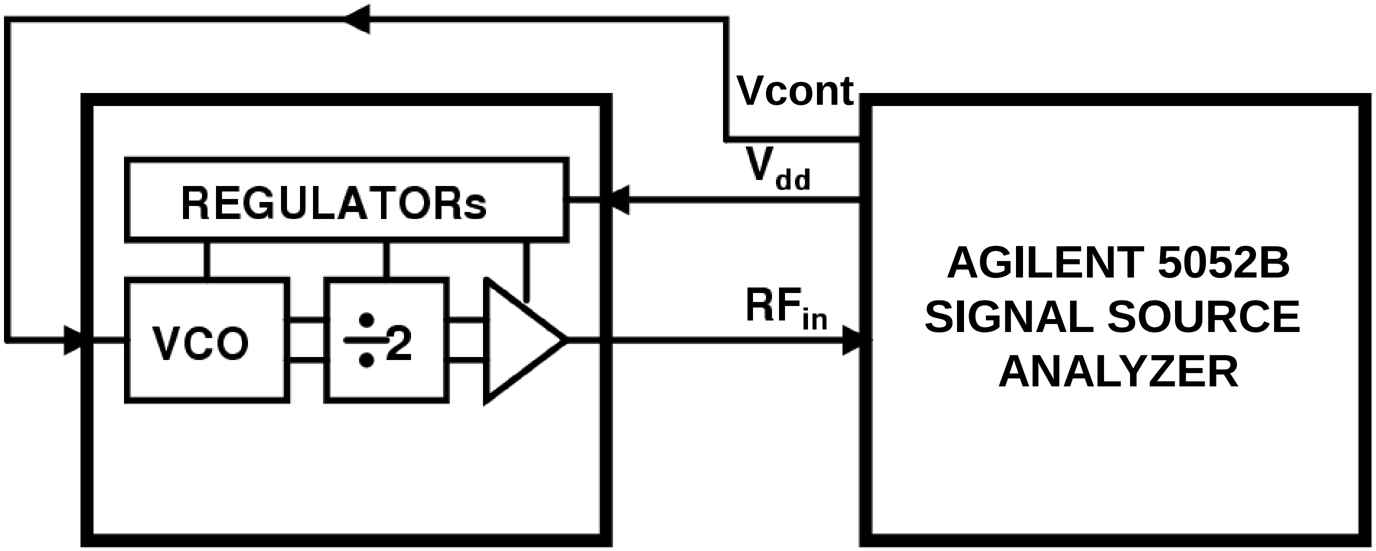
Example:
Cext = 0.22uF and R = 60k-ohm,
Without 1-shot pulse:
t = 13.2ms
With 1-shot pulse width of 14.4us:
t = 8.0us. (approx.)

VCO Layout



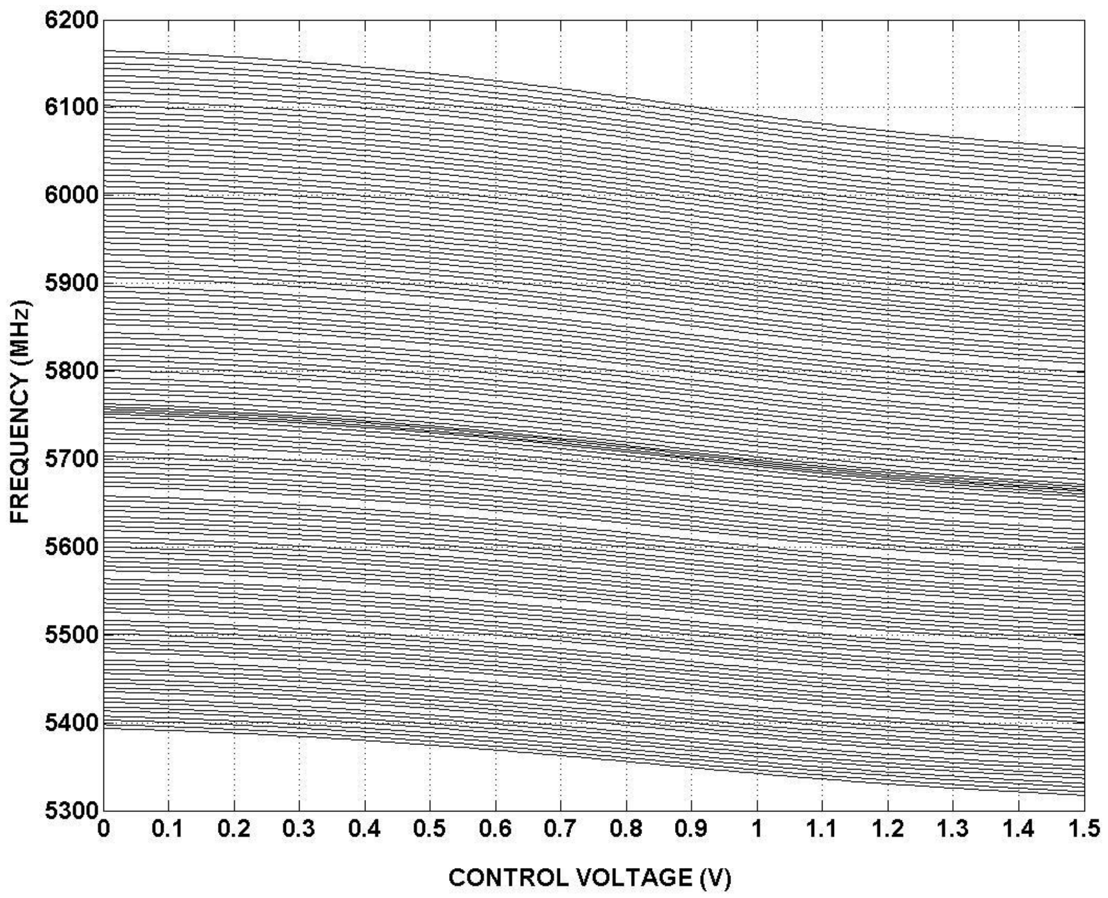
Chip Area = 460um x 300um

Measurement Test Setup



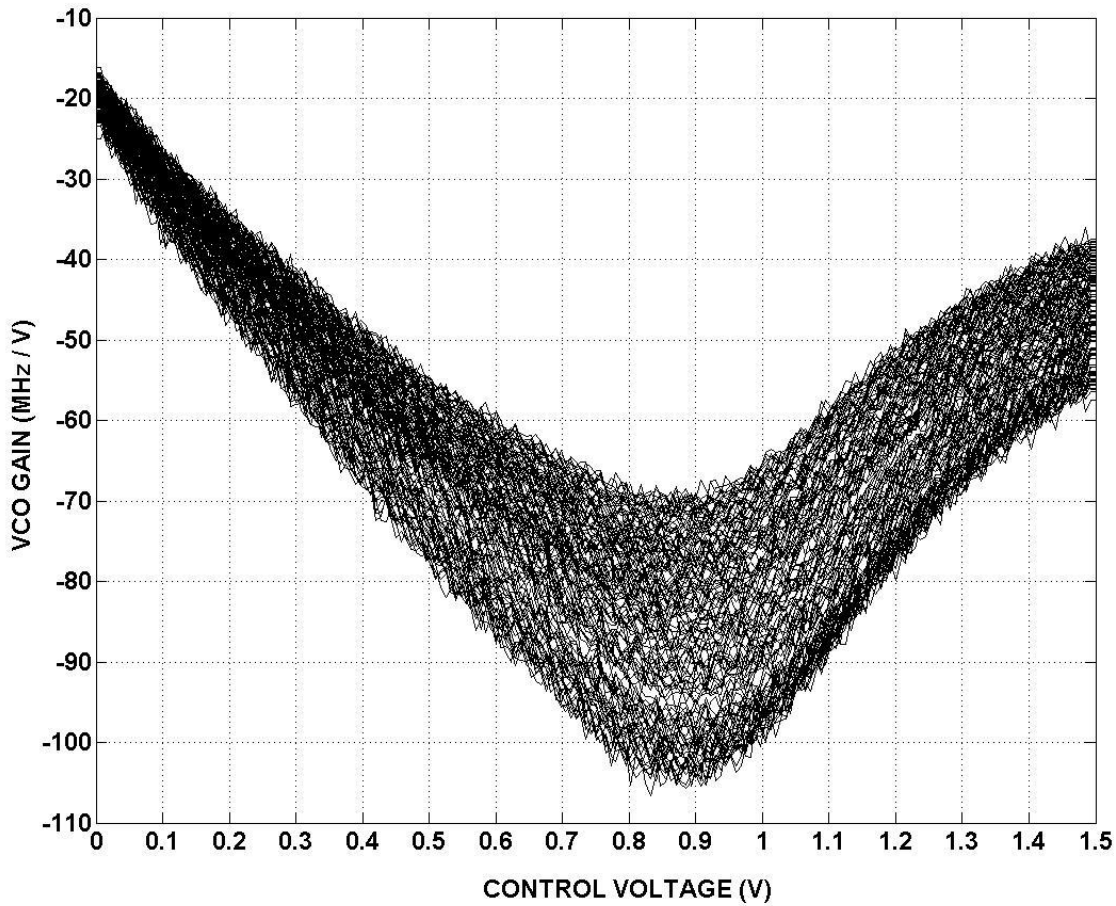
All VCO measurements were performed after divide-by-2 circuit

Measured Tuning (after div2)



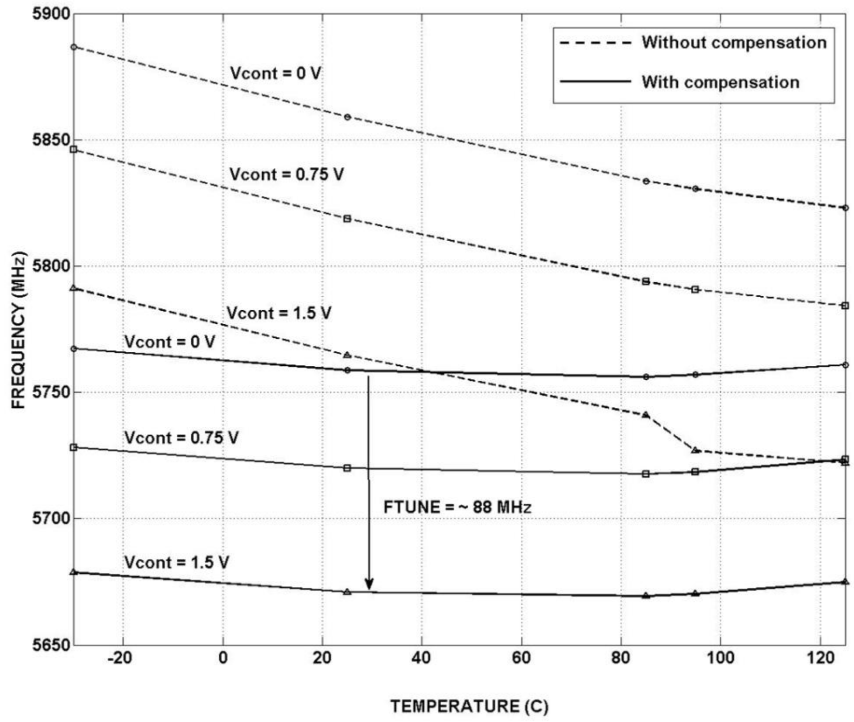
Frequency Coverage = 5034 MHz to 6200 MHz

Measured VCO Gain (after div2)



VCO Gain @ 0.8V = -75 MHz/V to -110 MHz/V

Measured Frequency Drift (after div2)



Worst case temperature drift:

-61.6 MHz without Compensation (T = -30 C to 125 C)

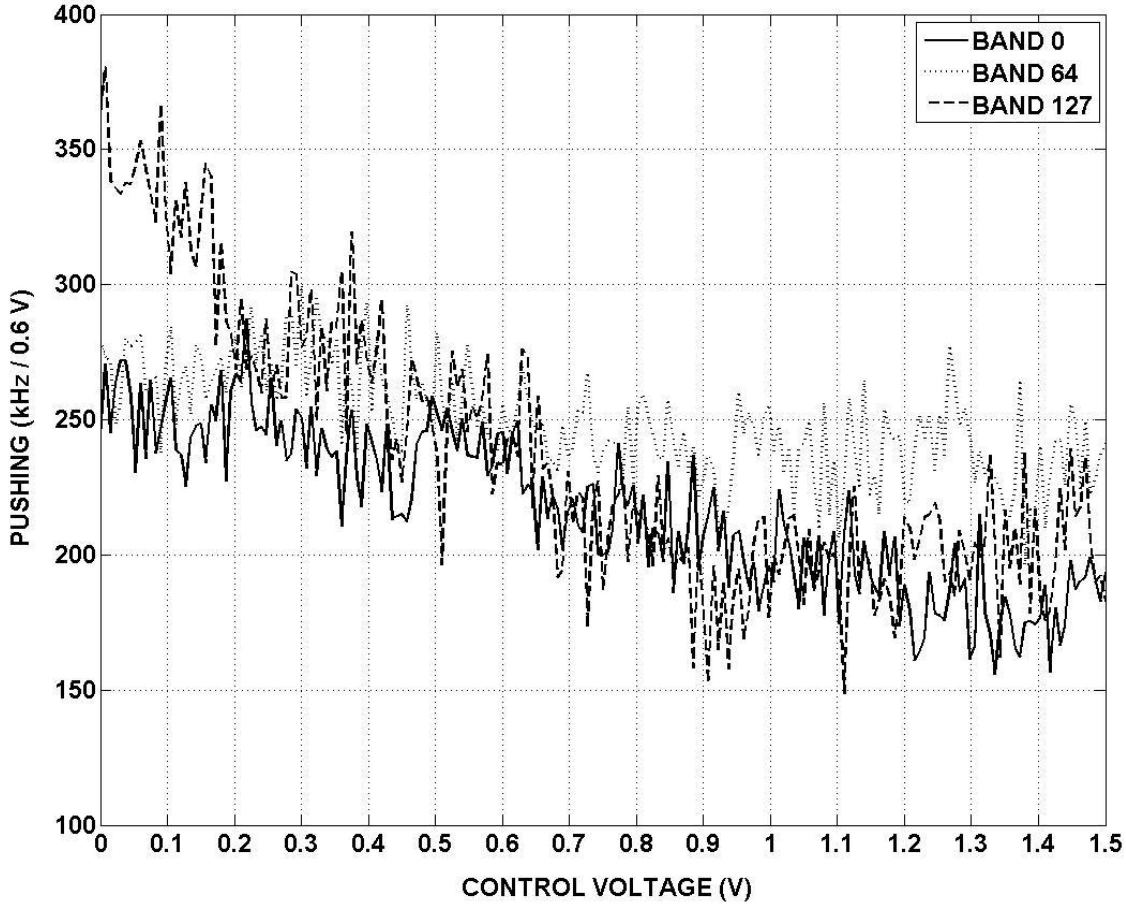
Almost Kvco=75MHz/V * (1.5V – 0.3V (vdstat of CP) – 0.3V (vdsat of CP) = 0.9V) = 67MHz

→ Problem

-10.5 MHz with Compensation (T = -30 C to 85 C)

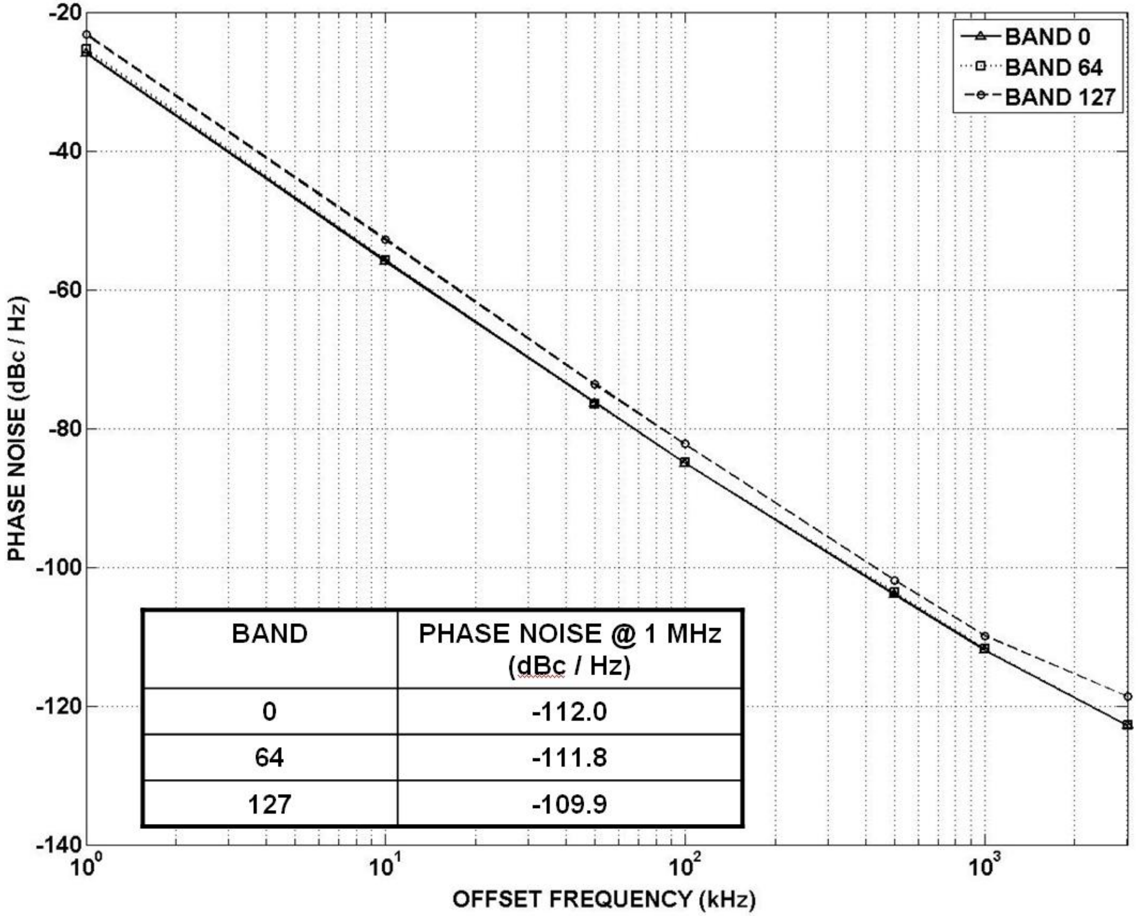
→ No problem

Measured Supply Pushing (after div2)



Worst Case Supply Pushing = 380 kHz / 0.6V

Measured Phase Noise (after div2)



BAND	PHASE NOISE @ 1 MHz (dBc / Hz)
0	-112.0
64	-111.8
127	-109.9

Phase Noise @ 1 MHz = -109.9 dBc / Hz

Summary

Technology	0.13 um CMOS
Supply Voltage	3.0 V - 3.6 V
Current Consumption (VCO)	21 mA
Frequency Coverage (VCO)	10.63 GHz – 12.33 GHz
VCO Gain @0.8 V (VCO)	-150 MHz / V to -220 MHz / V
Phase Noise @1 MHz (VCO)	- 103.9 dBc / Hz
Supply Pushing (VCO) [Vcc = 3.0 - 3.6 V]	760 kHz / 0.6V

Conclusion

- A 10 GHz frequency-drift temperature compensated LC VCO with fast-settling low-noise voltage regulator has been demonstrated.

Acknowledgements

- The authors would like to thank Scott Jorek, a former colleague, for many contribution on this project.