

# Audio Pre-Amplifiers for Digital Electret Microphones in 0.18 $\mu$ m CMOS Process

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**Abstract**—This paper presents CMOS audio pre-amplifiers with integrated voltage regulators for digital electret microphones. Several techniques for achieving high input impedance and proper input bias, as well as methods for implementing very low-frequency integrated high-pass filtering are presented. The amplifier with integrated high-pass filter has 14.8dB of specified voltage gain, 200 $\mu$ A of current consumption from 2.4V-3.6V supply, 60dB of total harmonic distortion, and 72.8dB signal to noise ratio at 1Vpp and 1kHz output.

## I. INTRODUCTION

Recently, there has been a lot of interest in audio pre-amplifiers for electret microphones in CMOS technology [1]-[3]. With today's ever increasing integration trends, a digital microphone has been proposed, which integrates an audio pre-amplifier and a 1-bit sigma-delta modulator together on a single chip [4]. With developments in MEMS microphones in CMOS technology [5], a fully monolithic digital microphone may soon become possible. With such a digital microphone only 4 interface pins are required, which include the ground, supply voltage, clock for sigma-delta modulator, and 1-bit digital output. Since most of today's signal processing is done in the digital domain, the 1-bit digital interface is not only convenient, but also has an advantage of being robust to any on-board noise or interference. Traditionally, audio pre-amplifiers have been realized using low noise JFETs [6]. The JFET has an advantage that when driven by a capacitive source like an electret microphone, it provides high input impedance and through its own leakage current conveniently self biases its gate to ground [6]. The capacitance of the microphone and high JFET input impedance realize a low-frequency high pass filter response. With the capacitance of the microphone on the order of a few pico-farads, an input resistance on the order of giga-ohms is needed to implement the corner frequency of less than 20Hz. Since JFET transistors are not available in standard CMOS technology, realizing this high input impedance is one of the design challenges. In addition, since the pre-amplifier must operate in audio frequency range minimizing 1/f noise is another design challenge in CMOS, as compared to a JFET pre-amplifier which does not exhibit large 1/f noise. Furthermore,

integration of low-frequency high-pass filtering with corner frequency less than 20Hz with good linearity is also a design challenge. This paper focuses on overcoming these design challenges and investigates three possible audio pre-amplifier architectures. First, a replica-bias based audio pre-amplifier is presented. Next, a replica-bias audio pre-amplifier with integrated low-frequency high pass filter is introduced. Finally, a replica-bias audio pre-amplifier with DC-servo based low-frequency filtering function is discussed. The paper concludes with measurement results.

## II. CIRCUIT DESIGN

A conceptual diagram of a digital microphone is shown in Figure 1. The system operates as follows. Sound pressure causes motion of the microphone membrane. Input network of the audio pre-amplifier provides high input impedance and biases amplifier input at the ground. Since capacitive microphone has a bias voltage of  $V_{dd}$  across it, motion due to sound pressure causes change in capacitance and  $I_{sound}$  current. The  $I_{sound}$  current is converted to voltage by the high input impedance realized by the back-to-back diodes  $D_1$  &  $D_2$  at the input of the amplifier. The pre-amplifier amplifies the voltage and its output is passed on to a sigma-delta modulator which produces a 1-bit sigma-delta modulated output. The voltage regulator and bias generator provide the voltage references and bias for the amplifier and sigma-delta modulator. The scope of this work includes only the audio pre-amplifier with integrated voltage regulator.

This paper investigates three amplifier architectures: a replica-bias based audio pre-amplifier AMP1 (Figure 2), a replica-bias based audio pre-amplifier with integrated additional low-frequency high pass filter AMP2 (Figure 3), and a replica-bias based audio pre-amplifier with DC-servo based low-frequency high pass filter AMP3 (Figure 4). Although the first high pass filter is implemented with the capacitance of the microphone itself and high input impedance of the amplifier, additional on-chip low frequency high pass filter is desirable to make the amplifier more robust to low frequency noise and interference.

The AMP1 replica-based audio pre-amplifier, shown in Figure 2, operates as follows. The input network consisting of resistors  $R_{ESD1}$  and  $R_{ESD2}$  and diodes  $D_1$ - $D_4$  performs the ESD protection function. These resistors limit the maximum current and the diodes provide the clamp needed to prevent the voltage at the input of the amplifier from exceeding the maximum allowable voltage. The input ESD network was designed for the 2kV human body model. The back-to-back diodes also provide the self-bias of the amplifier input to the ground and the high input impedance. The voltage regulator is designed for a 2V reference ( $V_{ref1}$ ). Transistors  $M_{P3}$ - $M_{P4}$  provide the voltage divider function and a 1V reference voltage as well as the reference bias current via  $M_{P2}$  for the source follower transistor  $M_{P1}$ . Non-inverting amplifier formed by the opamp  $A_1$  and resistors  $R_{A1}$ - $R_{A2}$  provides the required voltage gain that is designed to be 15dB. The opamp  $A_2$  is used as a buffer to provide low output impedance so that the gain depends only the resistor ratio of  $R_{A2}/R_{A1}$ . The DC level at the output of the amplifier is designed to be 1V when no input is applied. To minimize 1/f noise PMOS transistors were chosen.

The AMP2 pre-amplifier, shown in Figure 3, is similar to the AMP1, but adds a high-pass filter formed by capacitor  $C_{C1}$  and transistor  $M_{P4}$  which is biased in the triode-region. To improve linearity, the gate of  $M_{P4}$  is biased to the ground using the high-impedance network formed by  $M_{N1}$ ,  $M_{P5}$ , and  $C_{C2}$  so that the gate tracks the drain. The output of the amplifier is biased at 1V under no input condition. The voltage gain is also designed to be 15dB.

Figure 4 shows the AMP3 pre-amplifier, which achieves additional high pass function by using a DC-servo configuration. This technique is sometimes used in the wireless baseband filters for DC-offset removal [7]. The input network is the same as the other pre-amplifiers. The opamp  $A_1$  forms an inverting amplifier and the opamp  $A_2$  is a low output impedance buffer. Resistors  $R_{AT1}$ - $R_{AT2}$  form a voltage attenuator while the opamp  $A_3$  is a low output impedance buffer. The opamp  $A_4$ , capacitor  $C_{INT1}$ , and the triode resistors  $M_{INT1}$ - $M_{INT2}$  form an integrator. Since this integrator is connected in feedback, the amplifier closed-loop response has high pass characteristics. Transistors  $M_{PB2}$ ,  $M_{NB2}$ , and capacitor  $C_{C1}$  help to linearize the triode resistor  $M_{INT2}$ .

A folded cascode opamp with a PMOS input stage and conventional class-AB output stage is used [8], as shown in Figure 5. To achieve good high frequency power supply rejection ratio, compensation capacitors  $C_{PC}$  and  $C_{NC}$  are connected to the common-gate transistors  $M_{NB3}$  and  $M_{P4}$  [9]-[10]. The bias for the opamp is provided by a conventional constant-Gm bias circuit [11], which helps to maintain constant gain bandwidth product over supply and temperature variations. Figure 6 shows the schematic of the voltage regulator. The reference voltage is derived using the conventional bandgap reference [12]. The error amplifiers for the bandgap and regulator circuits also use folded-cascode opamps with PMOS input. Since the regulator and amplifier operate in the audio range, PMOS input opamps were chosen to minimize 1/f noise. To minimize 1/f noise further, resistor degeneration was used as well.

### III. MEASUREMENTS

The amplifiers described in the previous sections have been implemented in a standard 0.18um CMOS process. Figure 7 shows the layout image of one of the amplifiers (AMP2 type). The active chip area of AMP2 amplifier is 730um X 560um. The prototypes were packaged in a MTP-5 5-pin plastic package, and test on a standard FR-4 evaluation board. Figure 8 shows the measured frequency response of AMP2 amplifier, which shows a 3-dB corner frequency of 322 kHz. Despite on-chip low-frequency high-pass filter, the low-frequency response is still flat all the way to 20Hz which is the minimum frequency of the spectrum analyzer. The measured harmonic distortion of AMP2 amplifier is shown in Figure 9. The measured third harmonic distortion is -60dBc for a 1Vpp output and 1kHz input.

Measured results for all three amplifier architectures, (AMP1, AMP2, and AMP3) are summarized in Figure 10. All the amplifiers were functional from 2.4V to 3.6V as designed. The internal regulated voltage was measured to be 2V (within few milli-Volts) as shown in Figure 10. The DC voltage level at the opamp outputs was measured to be almost precisely 1V as designed. However, since AMP1 did not contain any additional on-chip filtering, as compared to AMP2 and AMP3, the 1V output voltage was sensitive to vibration and other disturbances. Due to the high input impedance, the recovery time from such disturbance was measured to be on the order of seconds and was easily observable on the oscilloscope. For these reasons, additional high-pass filtering function as implemented in AMP2 and AMP3 is needed for practical implementations of electret microphone pre-amplifiers. Measured current consumption for the AMP1, AMP2, and AMP3 amplifiers was 186uA, 200uA, and 236uA, respectively. Measured voltage gains were 14.8dB, 14.8dB, and 14.1dB for the three amplifiers, which is slightly smaller than our design target of 15dB. We suspect the discrepancy is due to the difference of the post-layout resistances as compared to the resistances used in our schematic simulations. While the measured harmonic distortion for AMP1, AMP2, AMP3 amplifiers was 65.6dB, 60.2dB, and 64.2dB, respectively, the measure signal to noise ratio was 74.3dB, 72.8dB, and 70.9dB, respectively. All harmonic distortion and signal to noise ratio measurements are reported for a 1Vpp output 1kHz sine wave.

Since AMP1 amplifier is susceptible to environmental disturbances and vibration pick-up it is not suitable for practical use. Although AMP3 amplifier, like AMP2 amplifier, is robust to environmental disturbances, it consumes the most current and achieves same or worse harmonic distortion and signal to noise ratio compared to AMP1 and AMP2 architectures. For this reason, on balance, AMP2 amplifier with integrated high pass filter achieves overall the best performance.

### IV. CONCLUSION

Techniques based on the back-to-back diodes for achieving high input impedance needed to implement very low-frequency high pass filter response and proper input bias were presented. Two approaches for implementing additional low-frequency on-chip high pass filtering were presented: one

based on linearized triode RC filter and the other based on DC-servo using linearized triode resistors. Finally, for comparison, measured results for three audio pre-amplifier architectures were presented.

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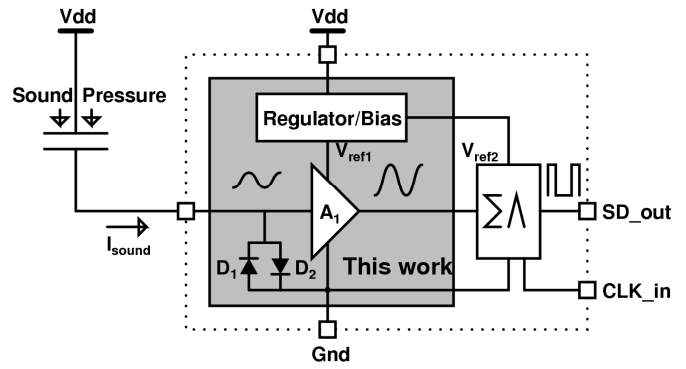


Figure 1. Conceptual diagram of an audio pre-amplifier for a digital electret microphone.

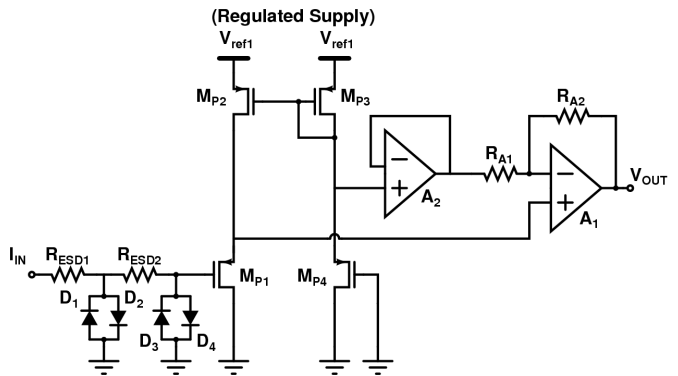


Figure 2. Realization of a replica-bias based pre-amplifier (AMP1) (no high-pass filter)

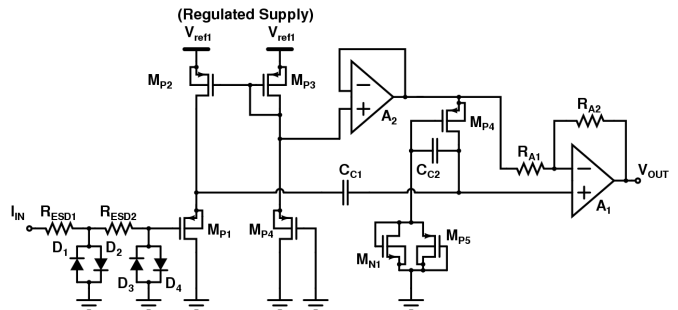


Figure 3. Realization of a replica-bias based pre-amplifier (AMP2) with very low frequency high-pass filter.

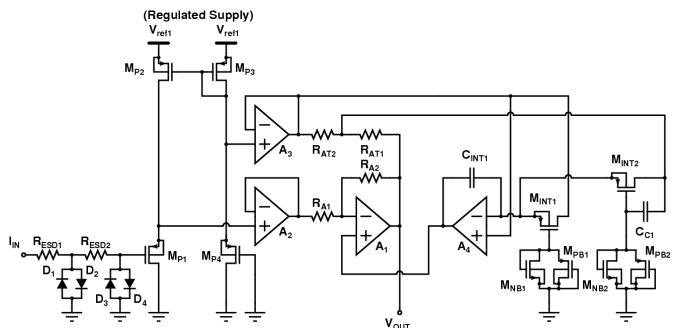


Figure 4. Realization of a pre-amplifier (AMP3) based on replica-bias with DC-servo high-pass filter.

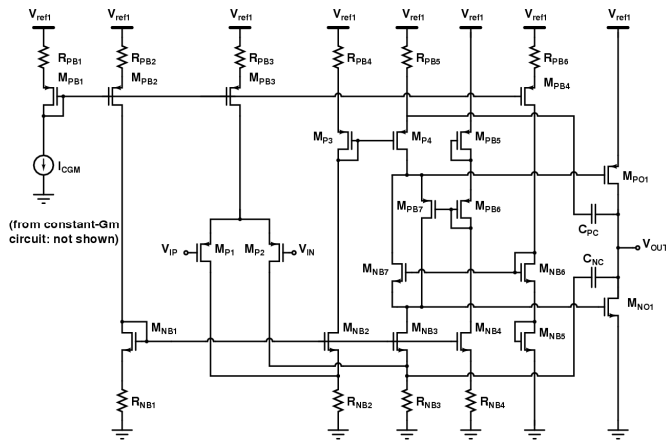


Figure 5. Folded cascode opamp with class-AB output stage.

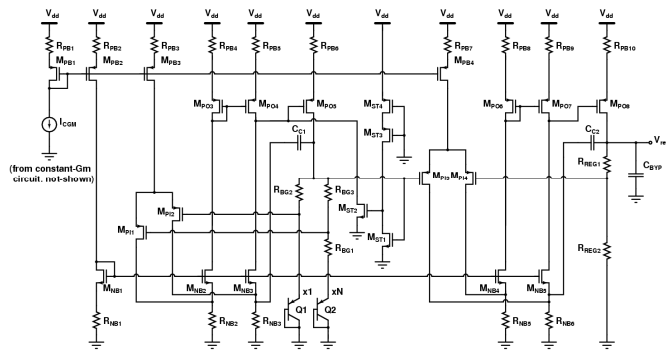


Figure 6. Voltage regulator (constant-Gm bias and secondary regulating amplifier not shown)



Figure 7. Chip layout for the pre-amplifier and regulator (for AMP2)

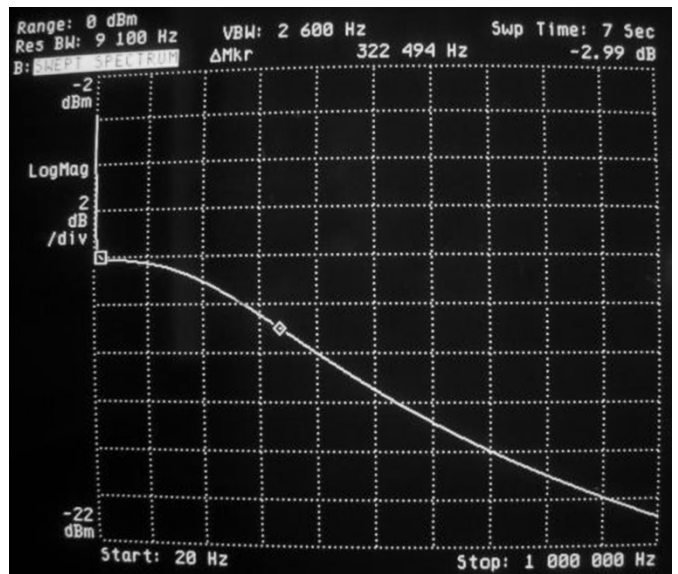


Figure 8. Measured frequency response (for AMP2)

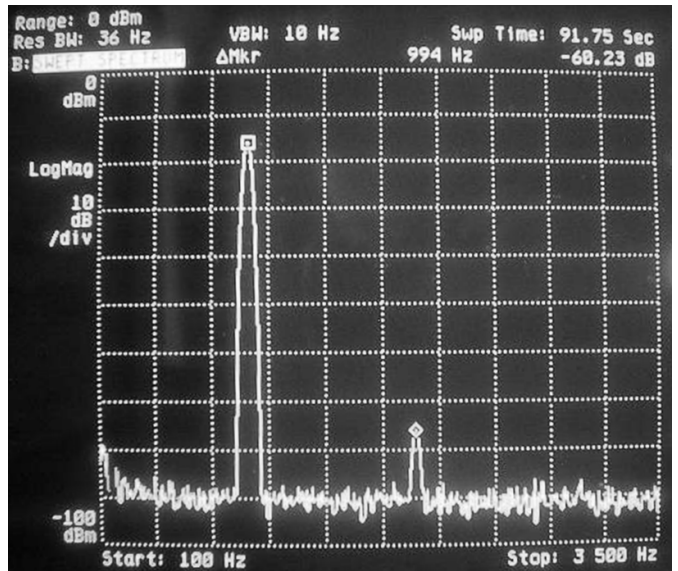


Figure 9. Measured output spectrum (for AMP2) when 1kHz input sinewave amplitude is set to produce 1Vpp at amplifier output.

Characteristics	Units	AMP1	AMP2	AMP3
Supply Voltage	Volts	2.4-3.6	2.4-3.6	2.4-3.6
Current Consumption	uA	186	200	232
Gain	dB	14.8	14.8	14.1
Corner Frequency	kHz	330	332	372
Reference Voltage	V	1.991	1.996	2.006
PSRR	dB	73	70.1	69.1
THD @1Vpp, 1kHz	dB	65.6	60.2	64.2
SNR @1Vpp, 1kHz	dB	74.3	72.8	70.9
Area	um	730x540	730x560	800x660

Figure 10. Measurement summary for the three amplifier architectures.