Wireless Innovation Without Bounds

Challenges and Design Considerations for Integrated VCOs in Wireless Communications

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Outline

- Introduction – Trends
- Basics – LC VCOs
- Issues and trade-offs of integrated VCOs
  - Will not cover various methods of low phase noise design
  - Will cover trade-offs that are not often covered in the literature.
- Modern fine-line processes: good or bad?
- Conclusions

Introduction

- Assumptions for this presentation: Integrated VCOs in ···
  - Wireless market
  - High volume market (cellular phone, tuners, WLANs, etc.)
  - LC VCOs

- SoC trend: High level of integration
  - Multiple standards in one chip (e. g., EDGE, WCDMA, LTE, etc.)
    - Widely different frequency ranges
    - Different requirements: low noise, low power, etc.
  - Multiple VCOs in a chip along with multiple LNAs, mixers, PAs, baseband blocks, micro-controller, etc.
- Process trends: CMOS
  - 0.18 um → 0.13 um → 90 nm → 65 nm → ···

Introduction – Underlying Theme

- "RFIC" design requires "analog" IC design skills.
- Modern CMOS process → many optional devices → more tools for engineers to innovate.

Basics

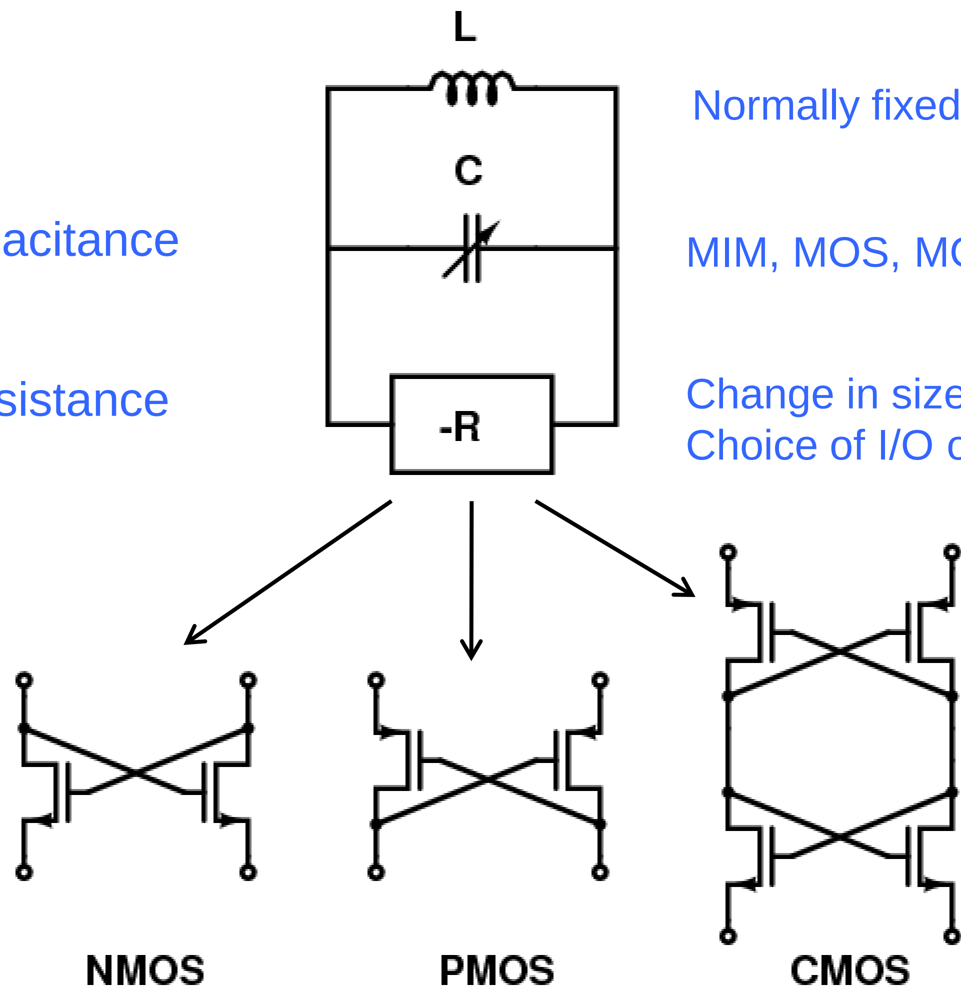
Basic Structures for LC VCO

Design Variables

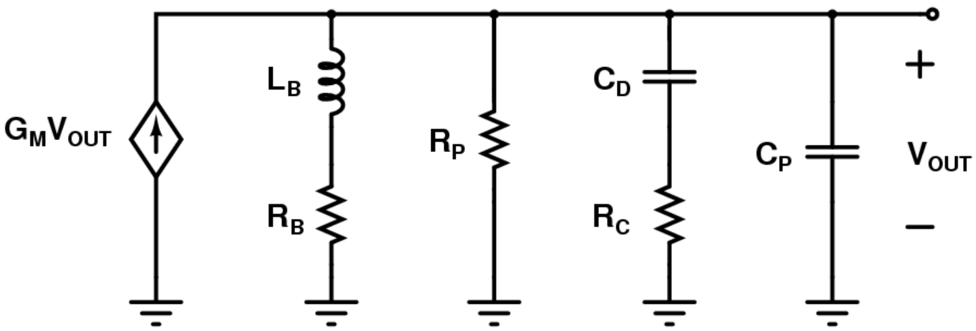
Inductance — Normally fixed

Variable capacitance — MIM, MOS, MOM, PNJ varactor, etc.

Negative resistance — Change in sizes or current; Choice of I/O or core devices



Basics: Conditions for Oscillations



Conditions for oscillations

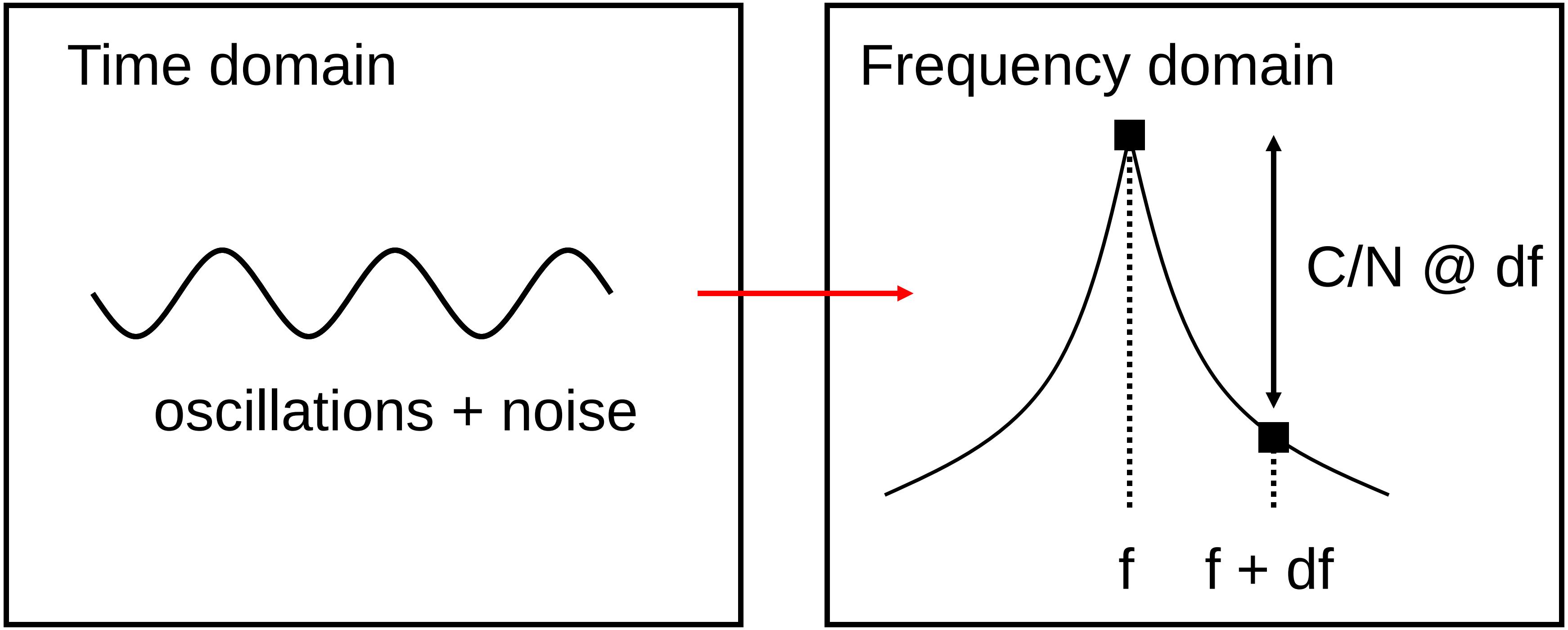
$$\omega_0^2 \approx \frac{1}{L_B \cdot (C_D + C_P)}$$

$$L(\omega_0) = G_M \cdot \left(Q_B^2 R_B \parallel R_P \parallel Q_C^2 R_C \right) \geq 1$$

This needs to be satisfied for PVT (process, voltage, temperature) variations with a margin !

Basics: Phase Noise

Phase Noise = Equivalent of a "Signal to Noise Ratio" for an Oscillator



Why is phase noise important ?
- Phase noise can affect receiver sensitivity (i.e. blocker + LO noise mix onto desired channel)

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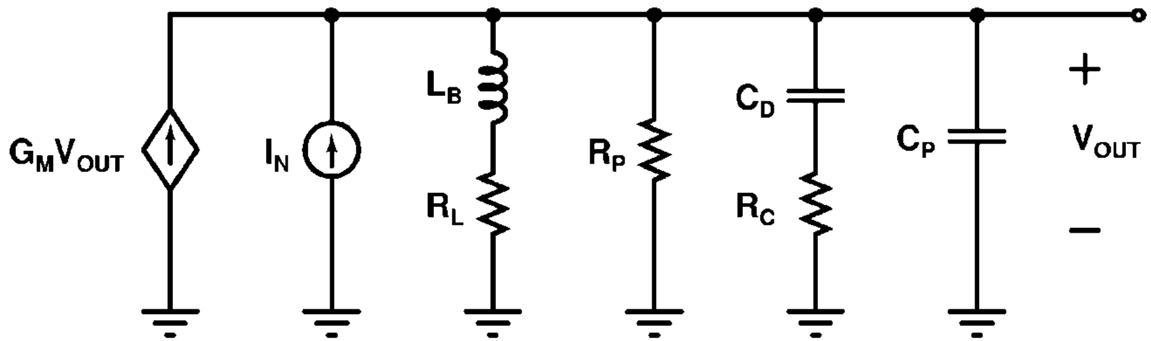
Basics: Phase Noise (linear model)

$$C_P = \gamma C_D$$



GM noise | loss in LC tank | -20 dB/dec

$$S_\theta(\delta\omega) = \frac{\frac{k_b T}{2} \times (1 + F_{GM}) \times \left(\frac{1}{\omega_0^2 (1+\gamma)^2 C_D^2 R_P} + R_L + \frac{R_C}{(1+\gamma)^2} \right) \times \left(\frac{\omega_0}{\delta\omega} \right)^2}{\frac{V_{out,peak}^2}{2}}$$

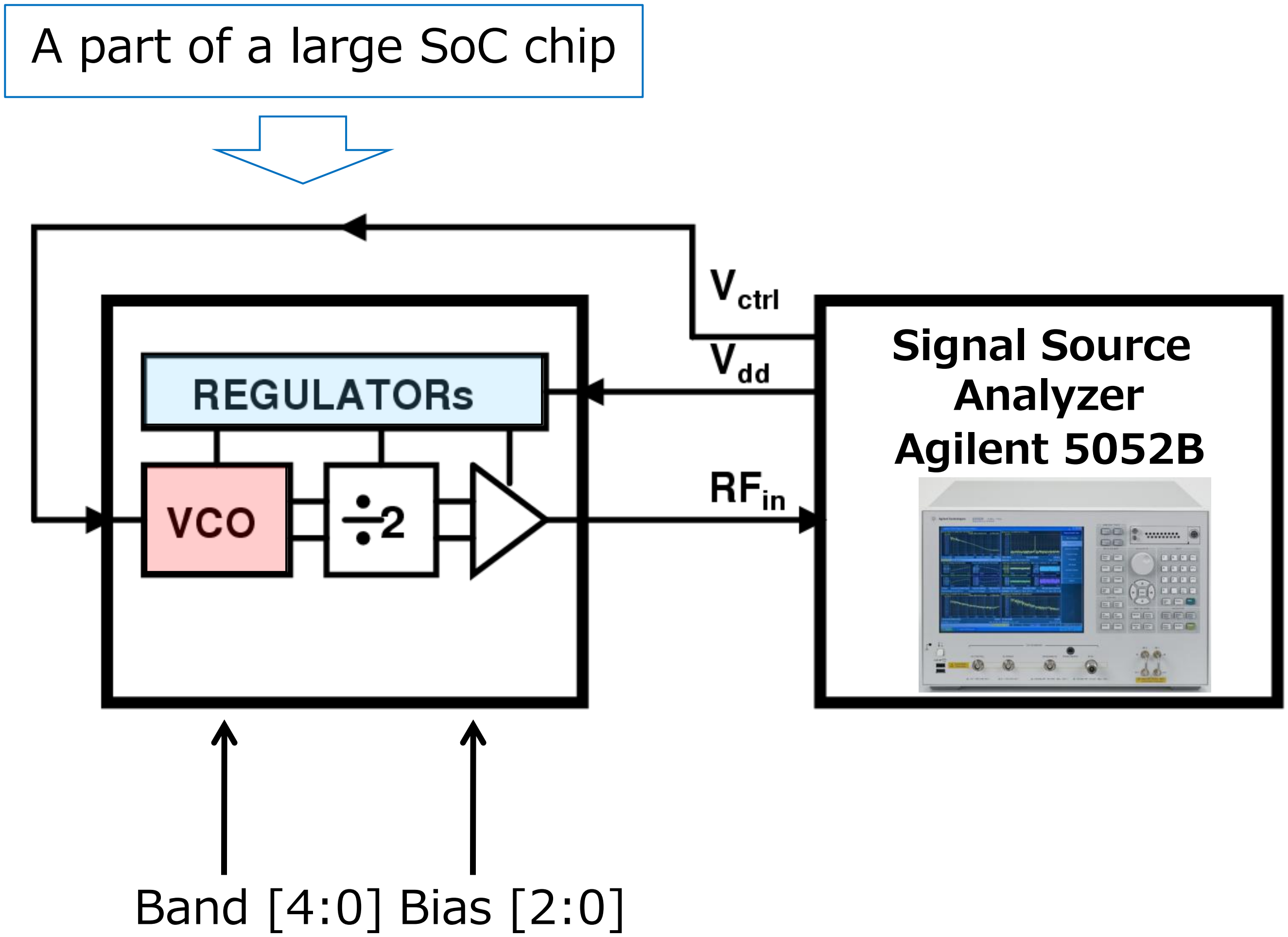
signal swing

How to get good phase noise?

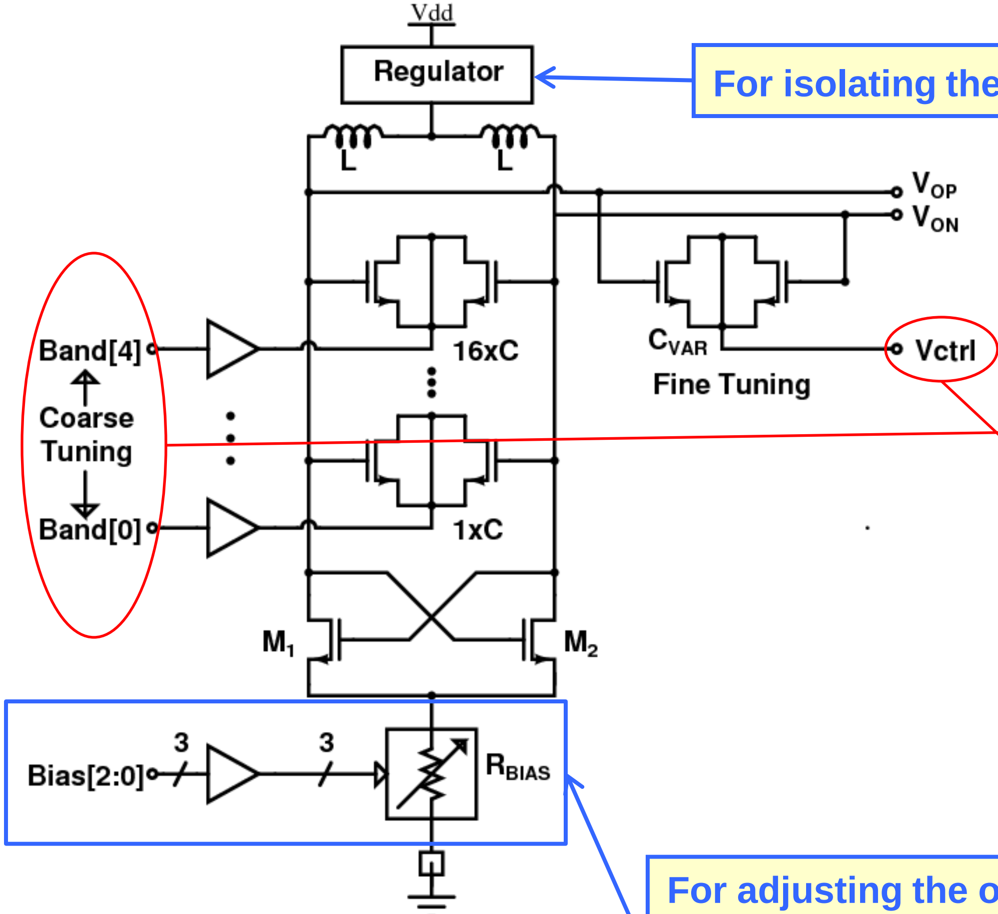
- Use high-Q devices if available
  - Thick metal for high-Q on-chip inductors
  - High-Q PN-junction and MOS varactors
- Very careful layout !!
  - High-Q layout vs. low parasitic capacitance layout
  - Try isolating the control lines
- Maximize oscillator voltage swing
- Care with the oscillation amplitude
  - Voltage limiting vs. current limiting

Case Study

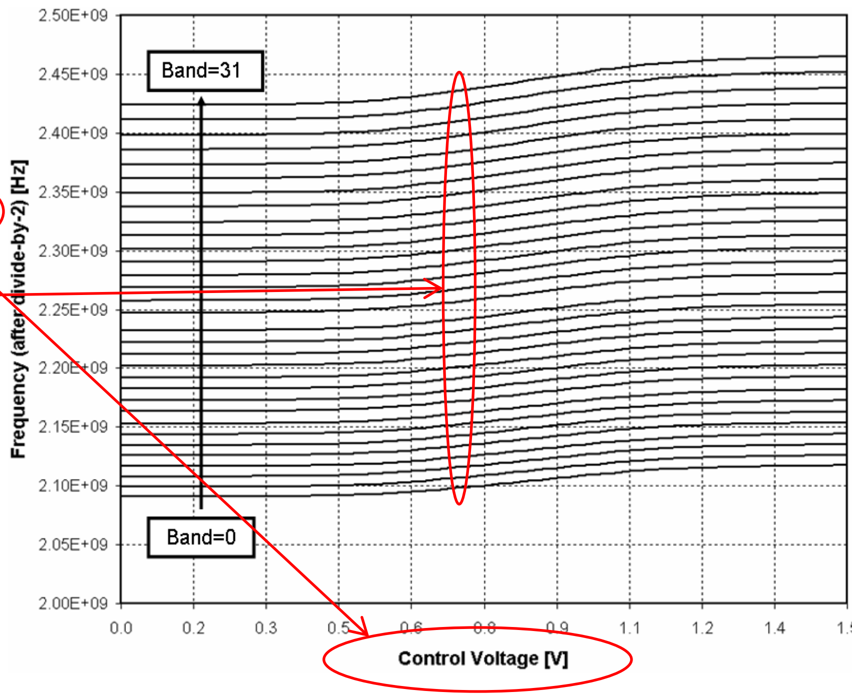
Measurement Setup



A Realistic VCO: A Simplified Regulated NMOS VCO



For isolating the VCO core from the supply disturbances

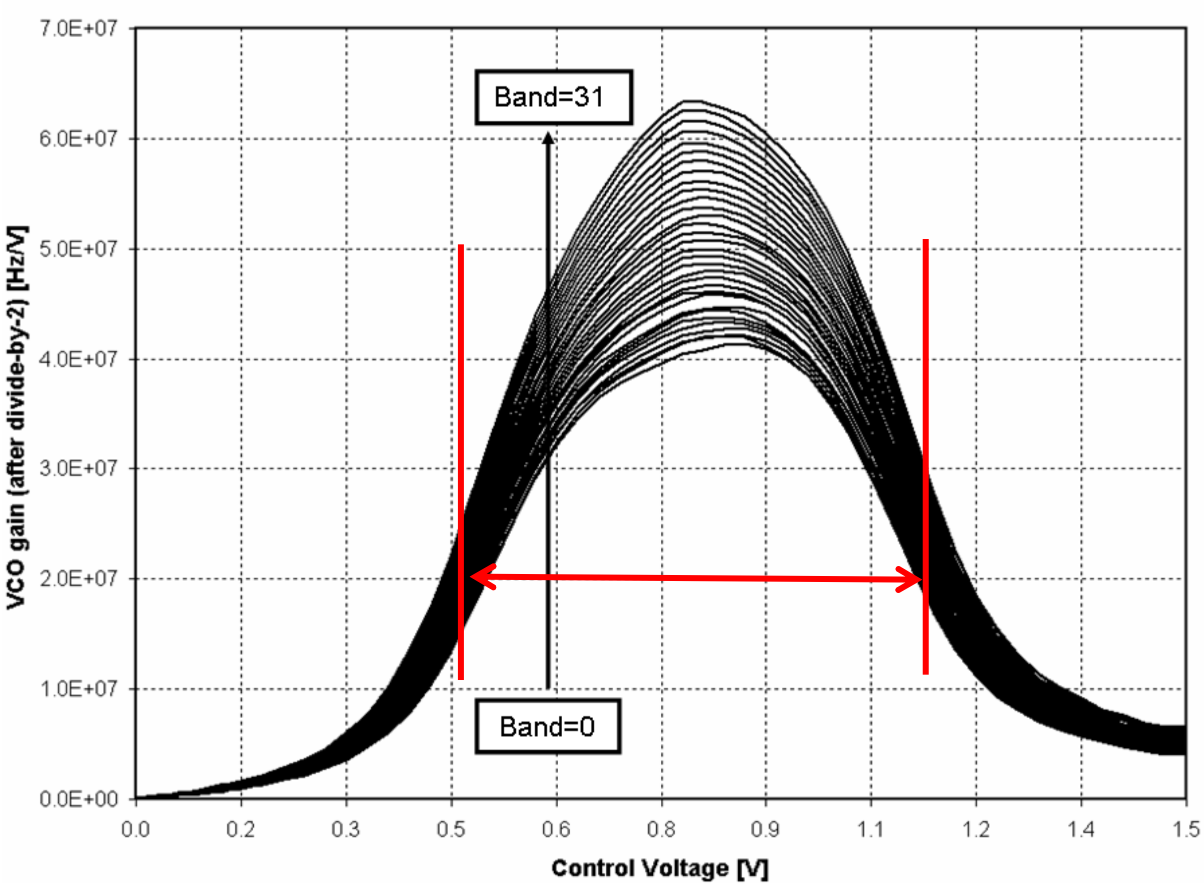


For adjusting the oscillation amplitude. It helps
- Robustness of oscillation
- Phase noise.

Use of resistors instead of current source → generally lower noise

A. Dec, et. al., "A 5 GHz LC VCO with extended linear range varactor in purely digital 0.15um CMOS process", 2009 IEEE RFIC Symposium

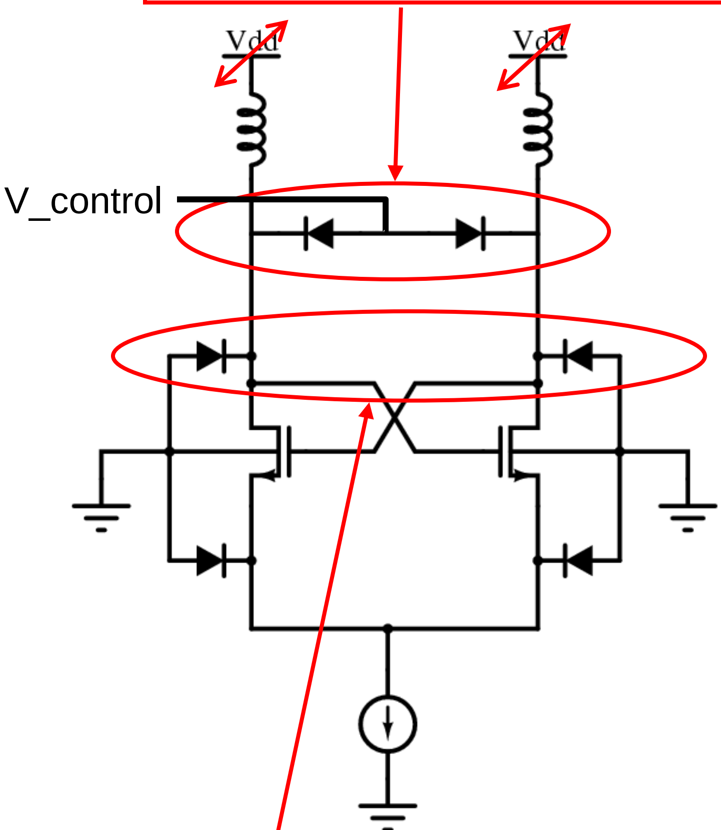
A Realistic VCO: Measured VCO Gain



VCO Gain @ 0.8V = 41MHz/V to 63MHz/V

Issue #1: Supply Pushing

Example: Varactors connected to Vcc



Example: Transistor diffusion diodes connect to Vdd.

Supply Pushing = Oscillation Frequency Sensitivity to Supply Voltage Variation

$$Supply\ Pushing = \frac{df_0}{dV_{CC}}\ [Hz/V]$$

Why is pushing important ?

- PLLs using VCOs with high pushing can un-lock when various parts of the system get enabled or disabled

Possible solutions ?

- PMOS based → less sensitive to Vdd variations
- Regulate the supply (Vdd)

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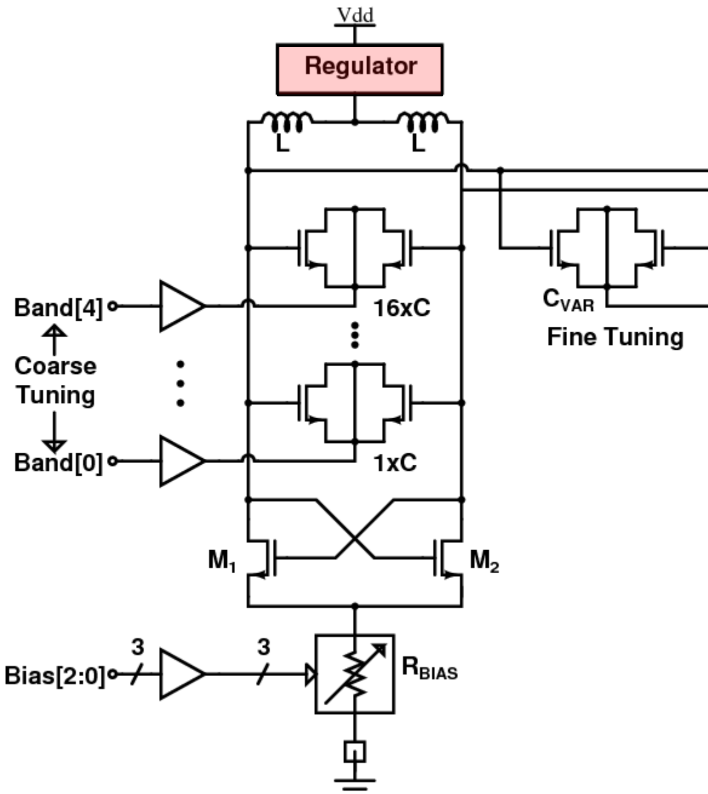
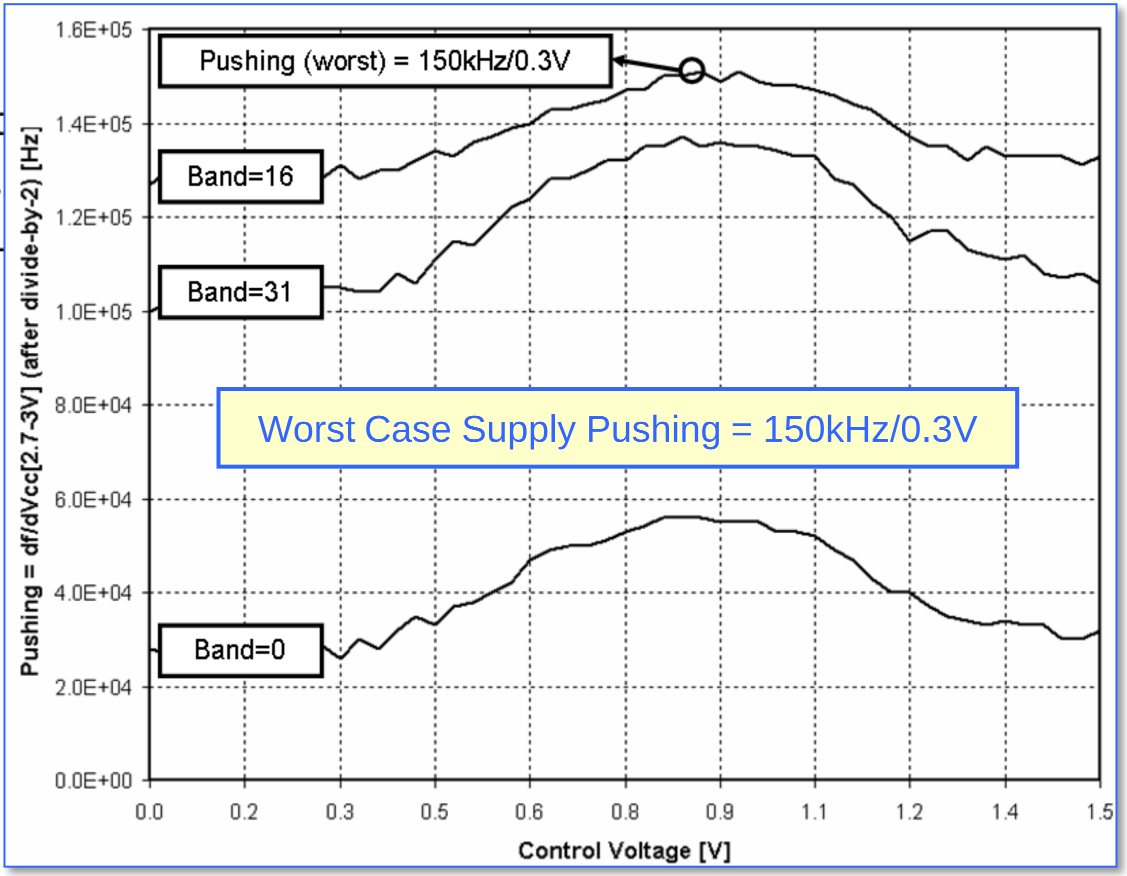
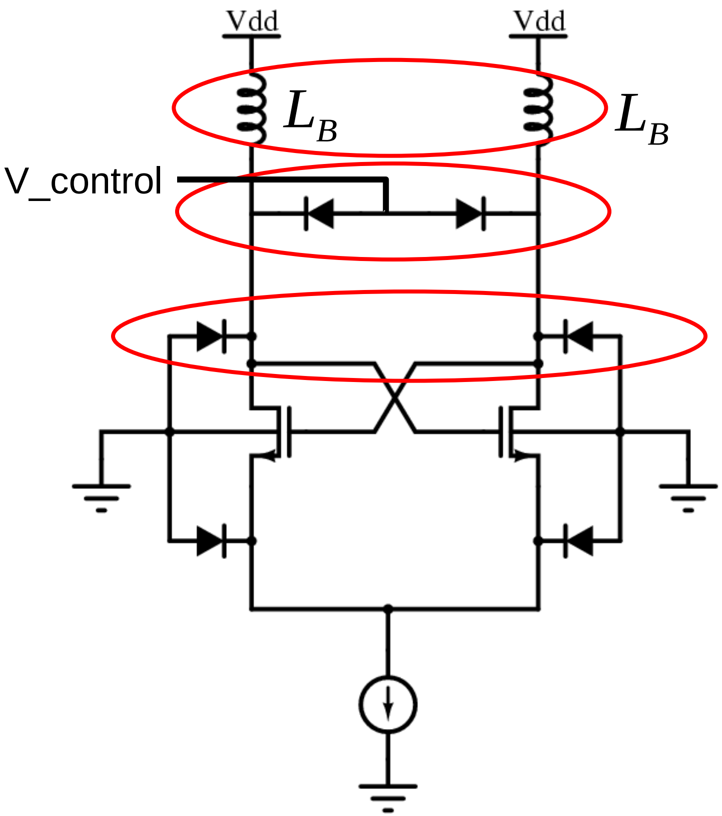
Issue #1: Supply Pushing: A Solution → Regulate Vdd





Issue #2: Temperature Variations

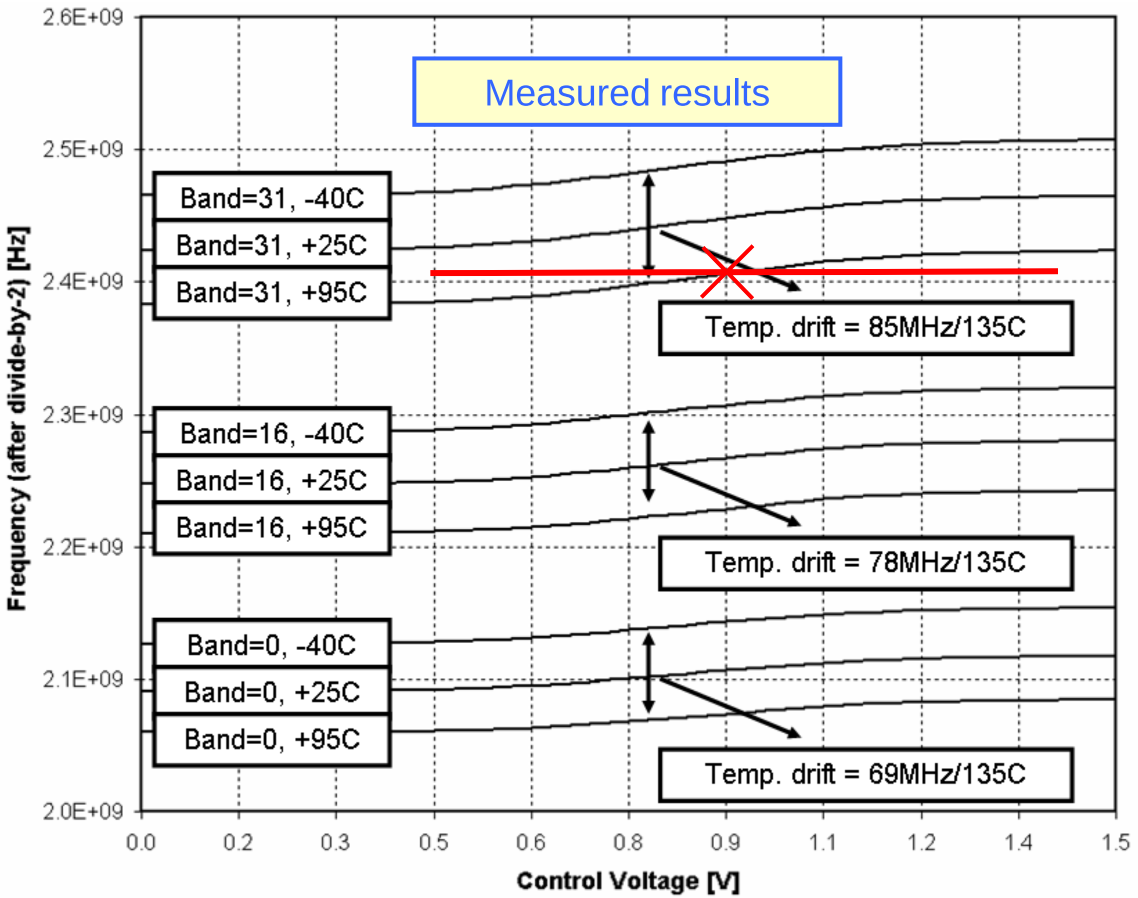
An Example



- Temp ↑ → the "capacitance" ↑
- When Q_B is small, the variation of Q_B affects the effective inductance value (L'_B)
  - Thus, the temperature dependence of the loss affects greatly.

$$L'_B = L_B\left(1 + \frac{1}{Q_B^2}\right)$$

Issue #2: Temperature Variations

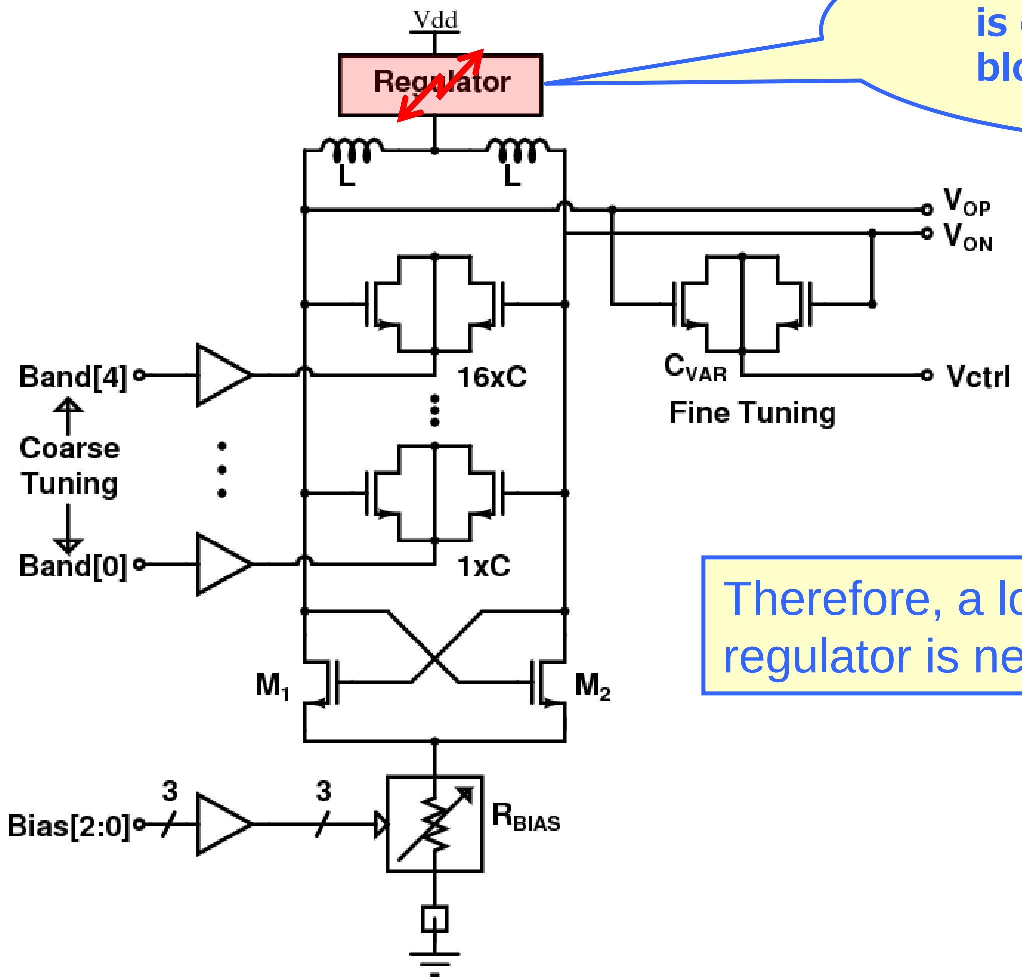


- Temperature behavior is difficult to simulate accurately.
- Need to model the temp. coefficient of inductor losses !

Issue #2: Possible Solutions

- Purposely embed a temperature dependence to the VCO control to reduce the temperature dependence.
- Increase Kv (VCO gain) to cover the temperature variations.
- Sense temperature change and adjust a fine-tuning varactor to negate the temperature variations.
- Do nothing if the system allows frequent auto-band calibration (for example, TDMA-type system)

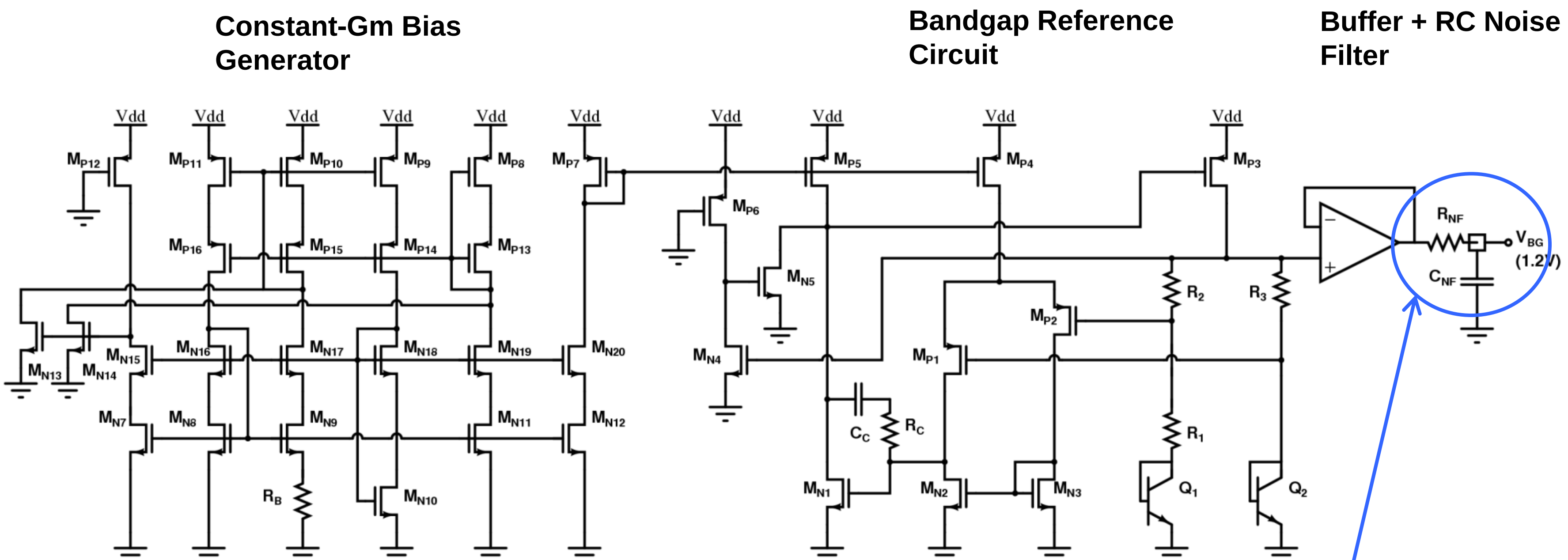
Issue #3: Regulator vs Phase Noise



Bandgap based regulator is often used. But, this block generates noise!!

Therefore, a low-noise bandgap based regulator is needed.

Issue #3: An Example Bandgap Circuit

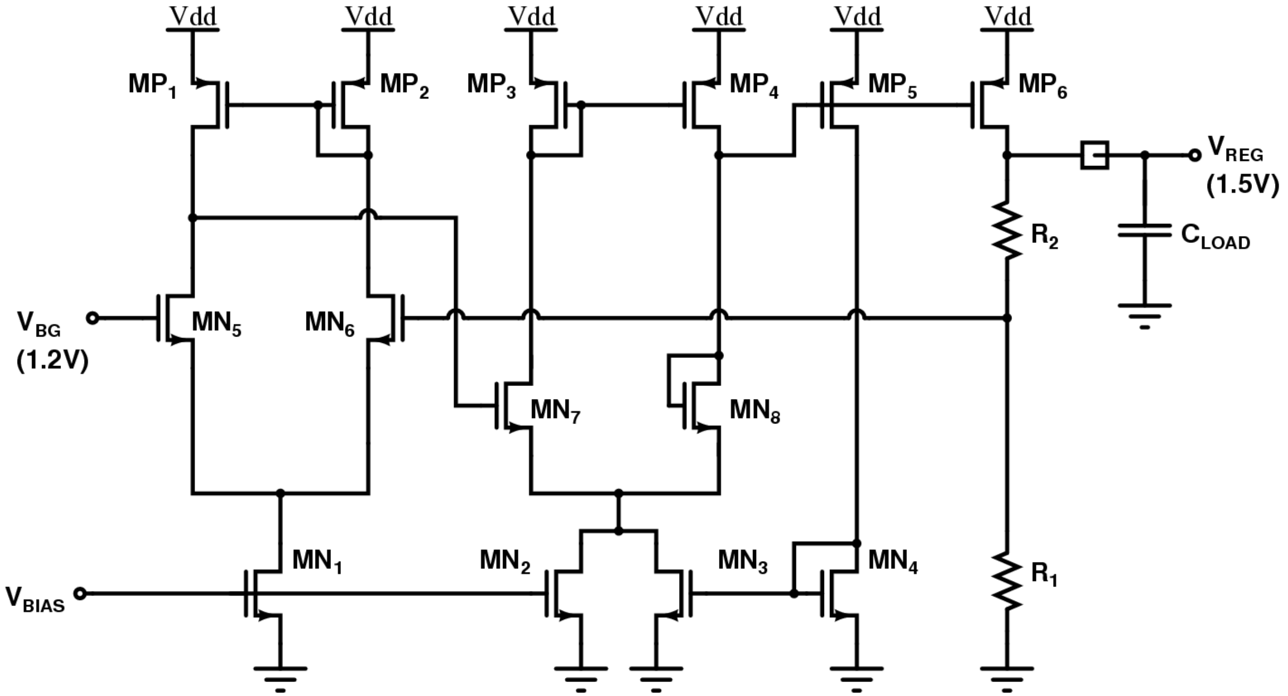


Noise filter to reduce bias noise impact on VCO phase noise

A possible problem → Slow turn-on → May need a speed-up circuit.

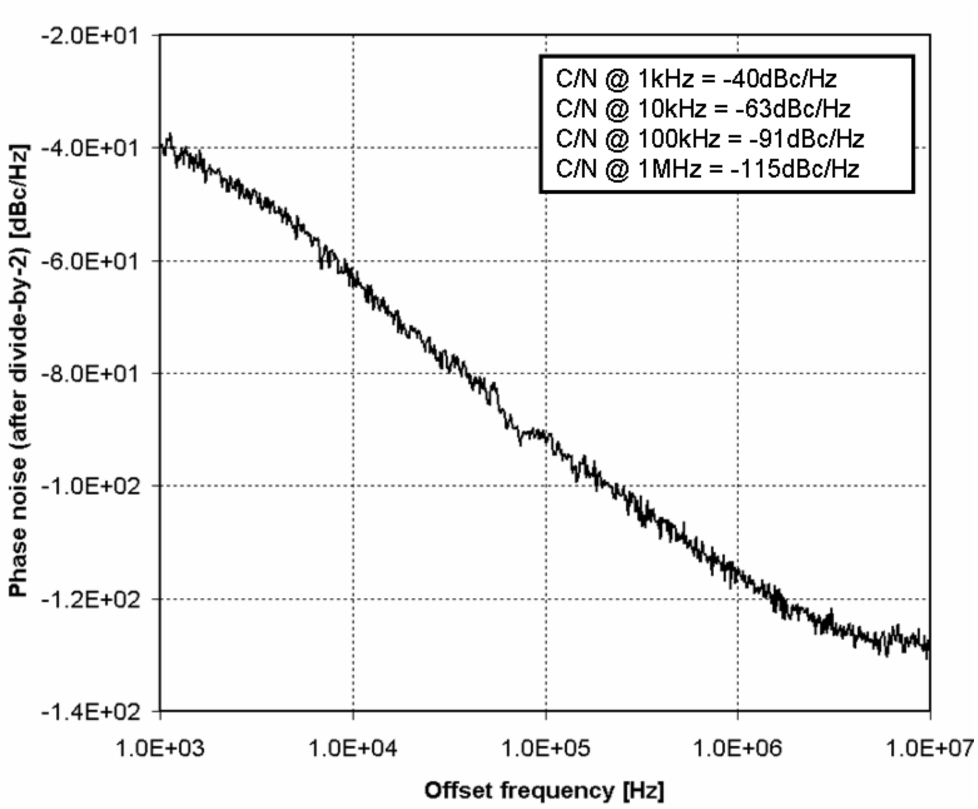
Analog IC design skill becomes essential.

Issue #3: An Example Voltage Regulator



Voltage regulator using external capacitor for good high-frequency PSRR

Issue #3: Measured Phase Noise



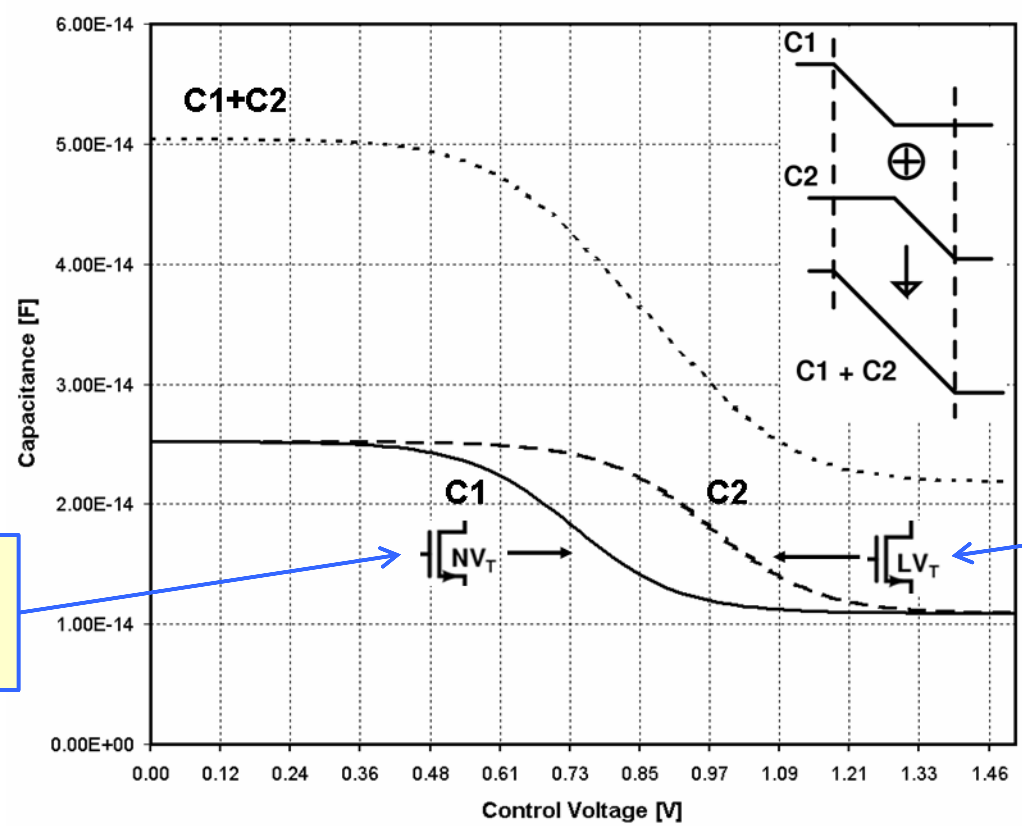
Phase Noise @ 1MHz = -115dBc/Hz

Modern Fine-Line Processes Good or Bad?

VCO Design: Modern processes: good or bad?

- Cons
  - Break-down voltage gets smaller but oscillation amplitude should be large for good phase noise.
  - 1/f noise is often larger.
- Pros
  - Faster devices.
  - Tuning range increases.
  - A variety of devices such as native devices, devices with different threshold (normal, low, etc.) are available.
    - More “tools” for engineers to innovate !

Issue #4: Linear Range Extension: An Example Use of Device Options

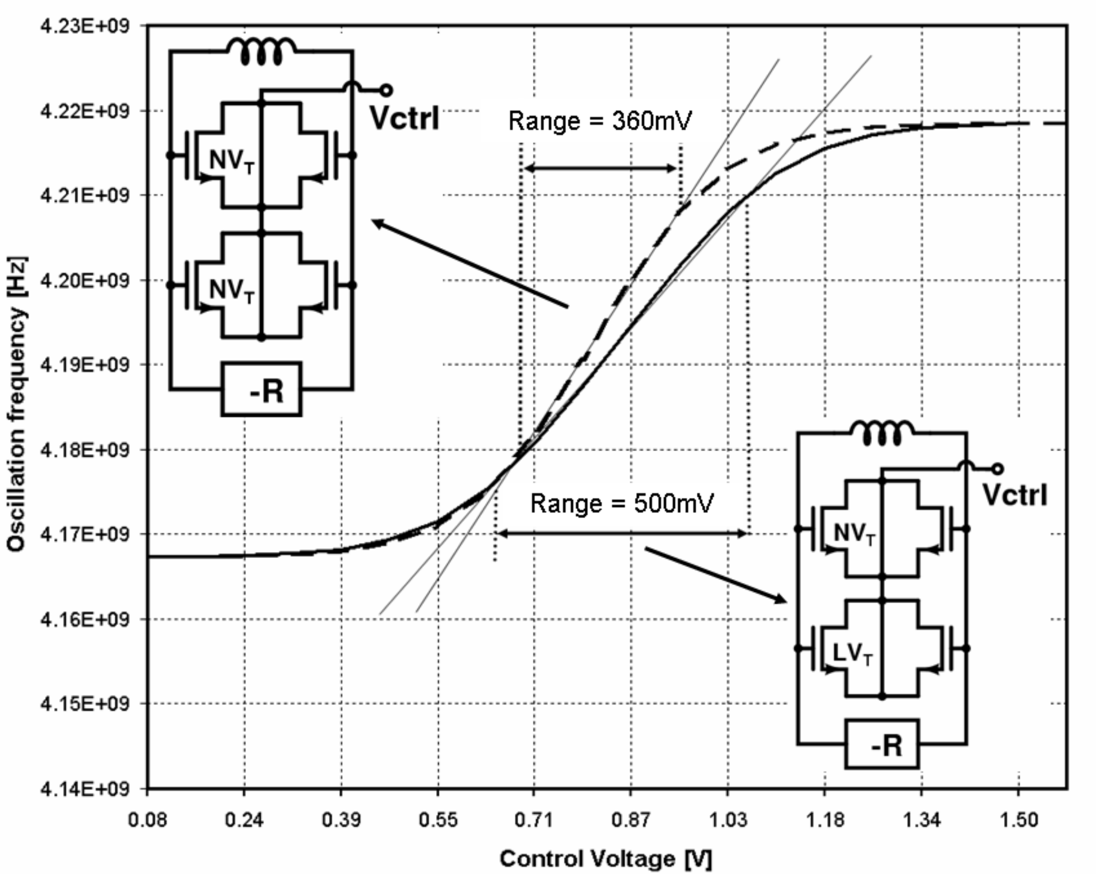


Normal Threshold Device

Low Threshold Device

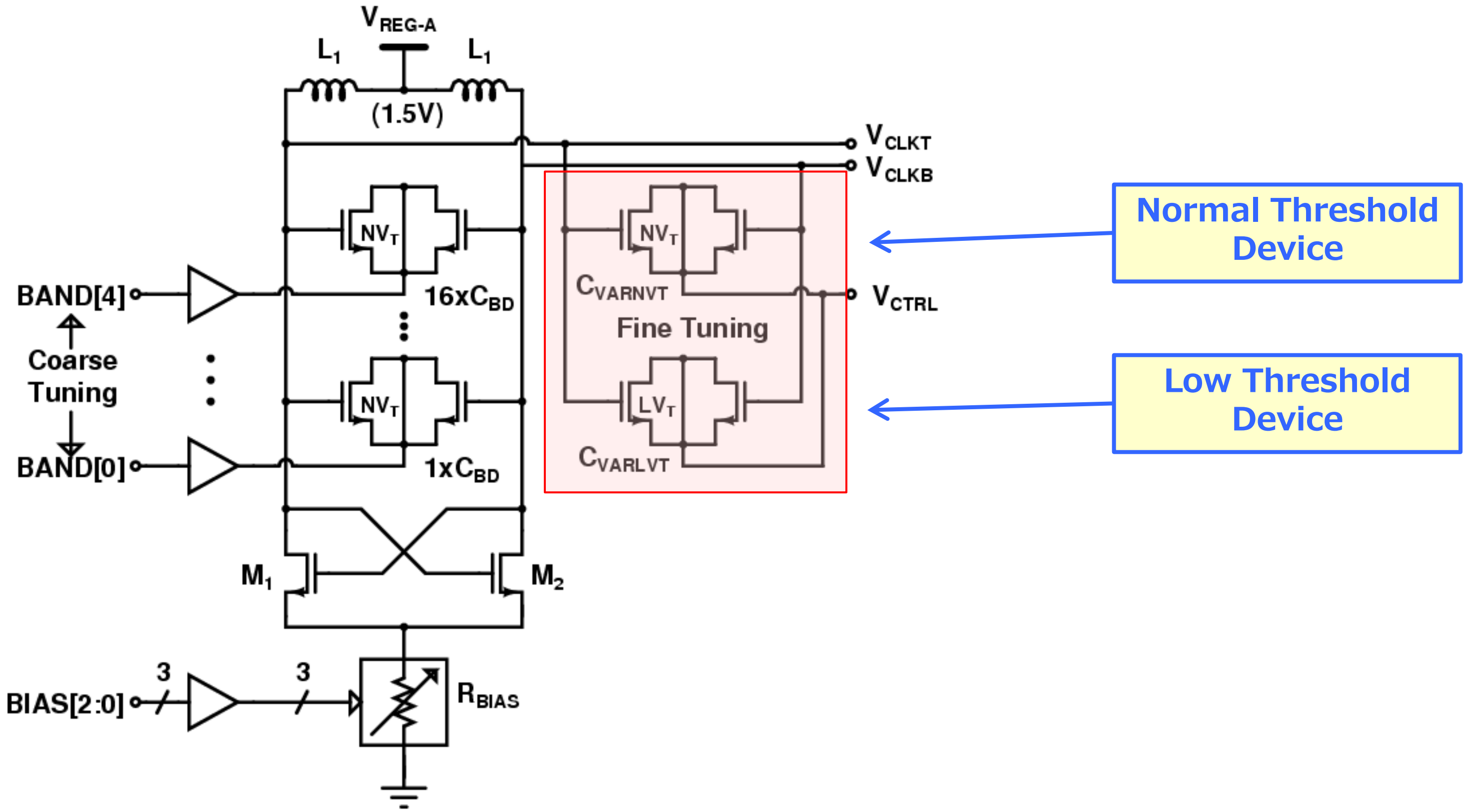
Possible to linearize MOS capacitance by superposition of normal & low threshold transistors

Simulated Range Extension



Linear tuning range improvement of 38%

VCO Schematic using the Range Extension



Conclusions

- ❑ Modern transceiver ICs require multiple VCOs integrated on chip.
- ❑ Complex trade-offs exist among oscillation frequency, Kv (VCO gain), required frequency coverage, supply pushing, phase noise, power, area ($), PVT variations, startup time, etc.
  - ❑ The trade-offs get more complicated as the process shrinks.
- ❑ Modern processes provide various options for active and passive devices → More "tools" for engineers.

- ❑ Therefore, more room for engineers to innovate !

Acknowledgment

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