A 5GHz LC VCO with Extended Linear Range Varactor in Purely Digital 0.15um CMOS Process

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Motivation

- Objective: To design a 5GHz LC-VCO in purely digital CMOS process

- Challenges:
  - No RF components in the design kit
  - No thick metal (low-Q inductors)
  - No MIM-capacitors
  - No Varactors – only MOS transistors available
    - Custom PN-junction & accumulation varactor layout possible, but DRC / LVS / Device Models not supported
    - MOS inversion C(V) characteristic modeled accurately, but highly non-linear -> linear-region extension desired

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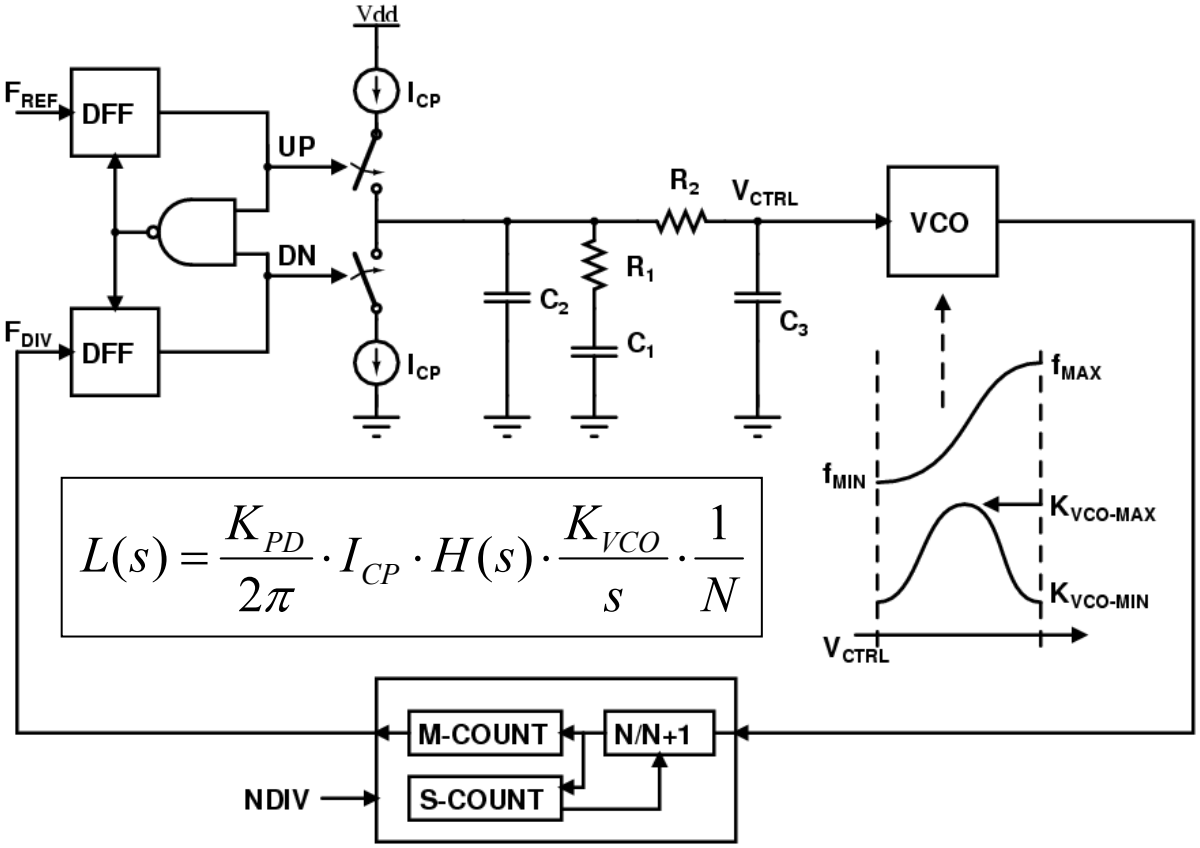
PLL & VCO Tuning



$$L(s) = \frac{K_{PD}}{2\pi} \cdot I_{CP} \cdot H(s) \cdot \frac{K_{VCO}}{s} \cdot \frac{1}{N}$$

VCO Gain and hence PLL loop gain & phase margin vary with V_{CTRL} -> therefore it's desirable to keep VCO tuning characteristics as linear as possible

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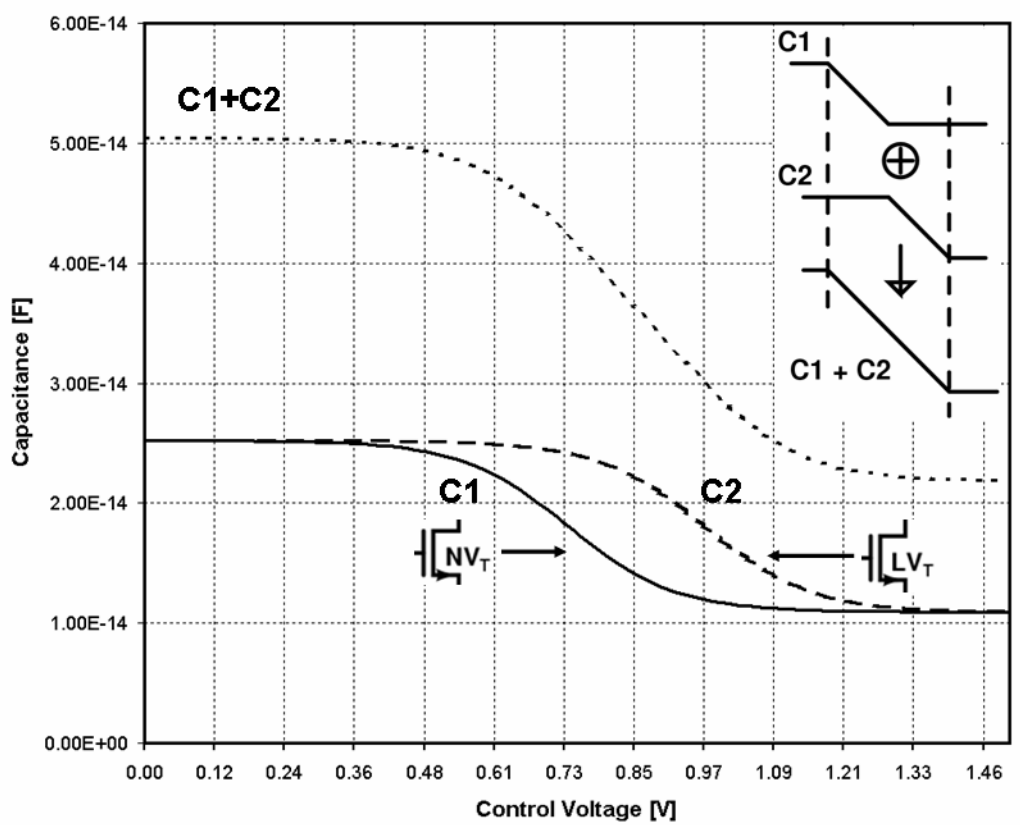
Range-Extension Concept



Possible to linearize MOS capacitance by superposition of normal & low threshold transistors

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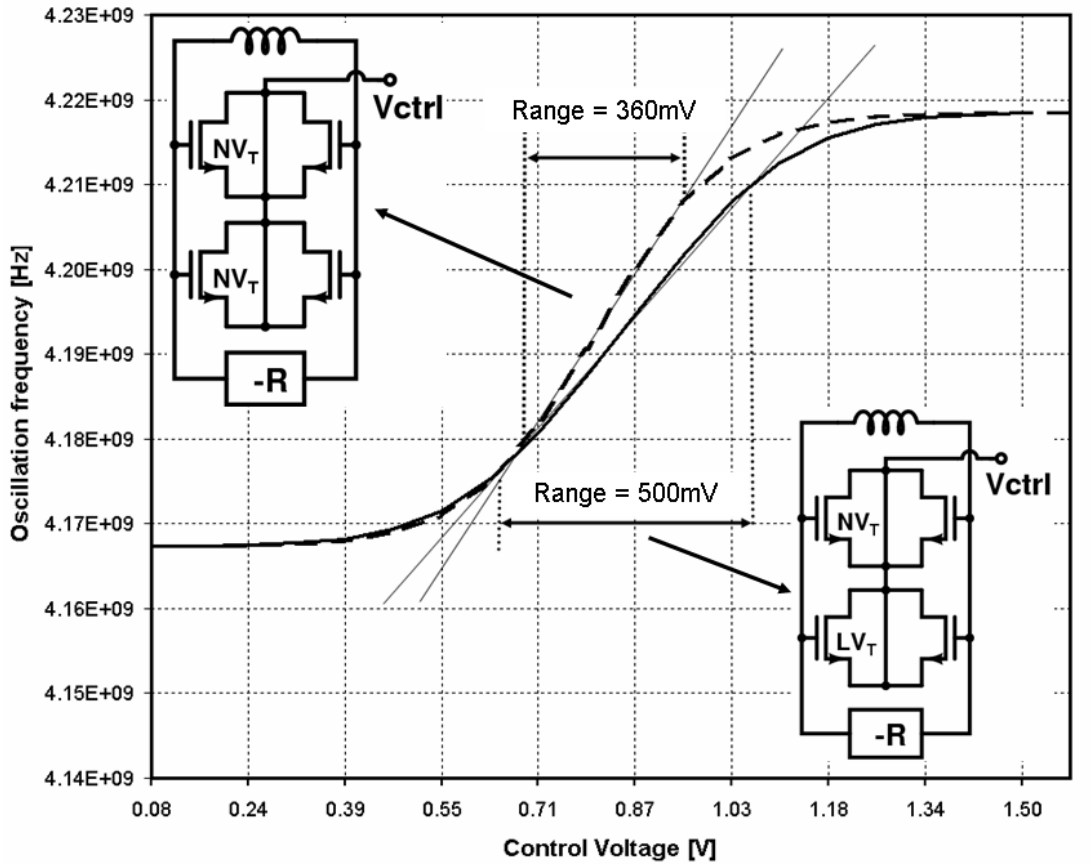
Simulated VCO Range Extension



Linear tuning range improvement of 38%

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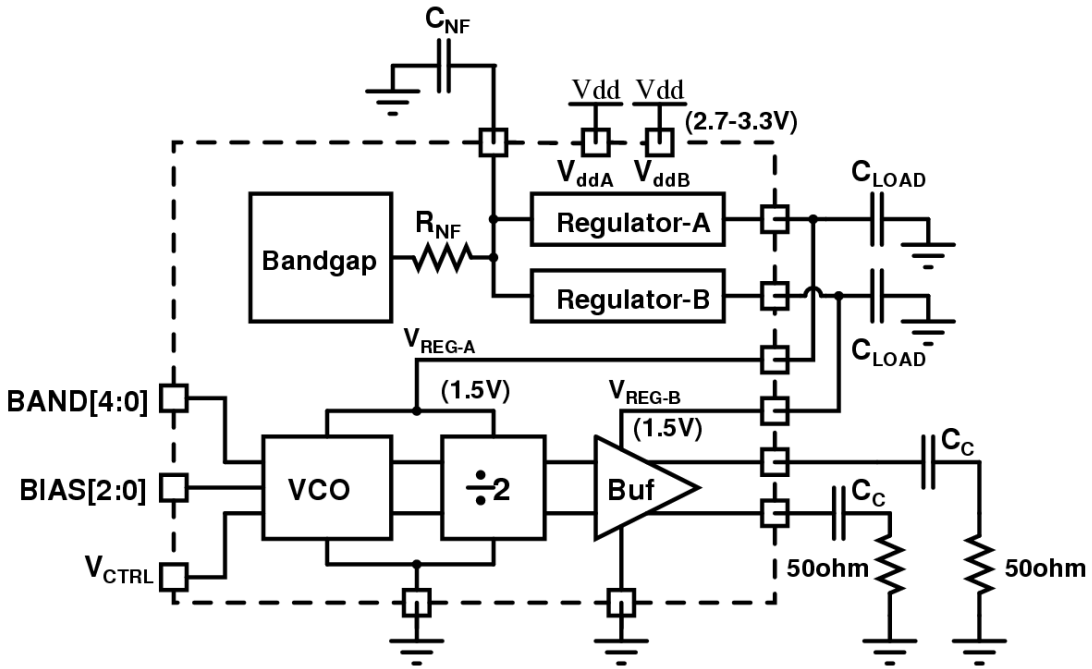
Test Chip Diagram



- Low noise regulators using noise filter for good VCO pushing
- Frequency divider because final application need 0/90 degree phases
- Output buffer to drive a 50-ohm measurement equipment

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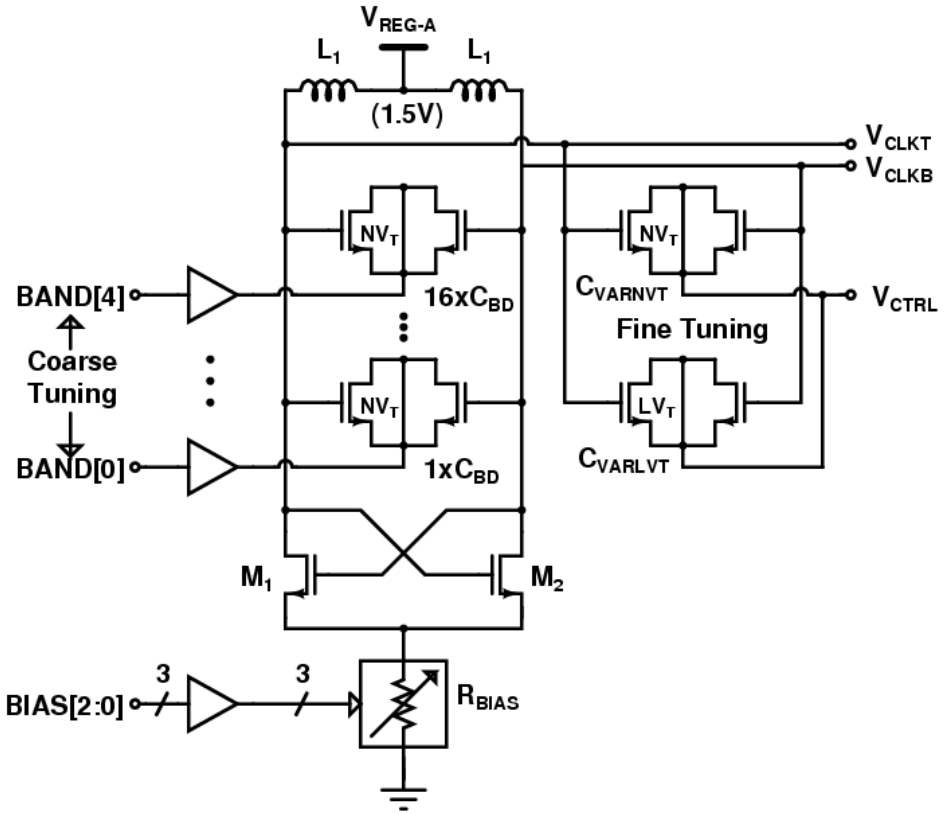
VCO Schematic



- NMOS-capacitor has high-Q
- NMOS-capacitor must be biased to the supply
- NMOS LC VCO best choice
- VCO bias 3-bit programmable for phase noise optimization

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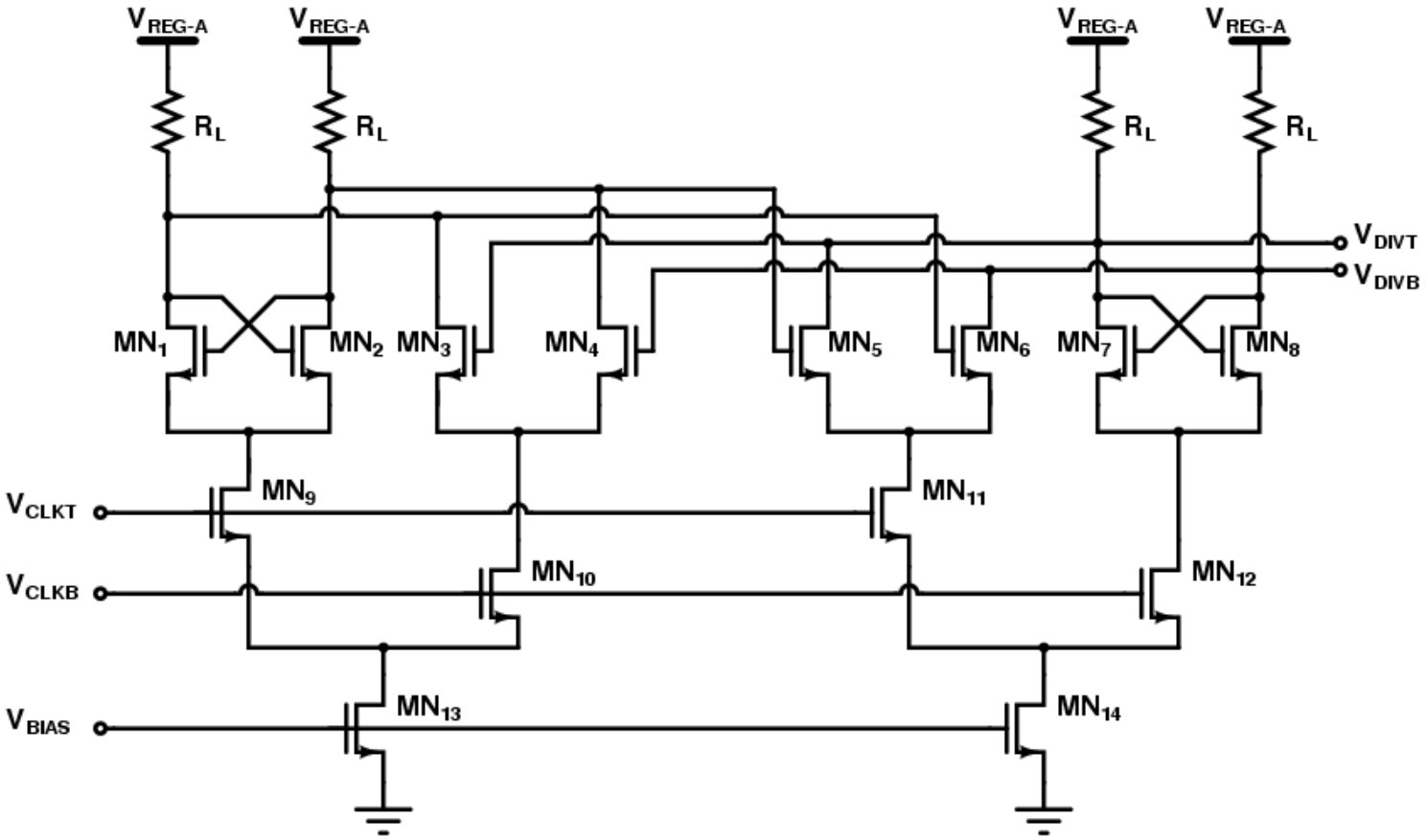
Divider Circuit



Conventional CML divider

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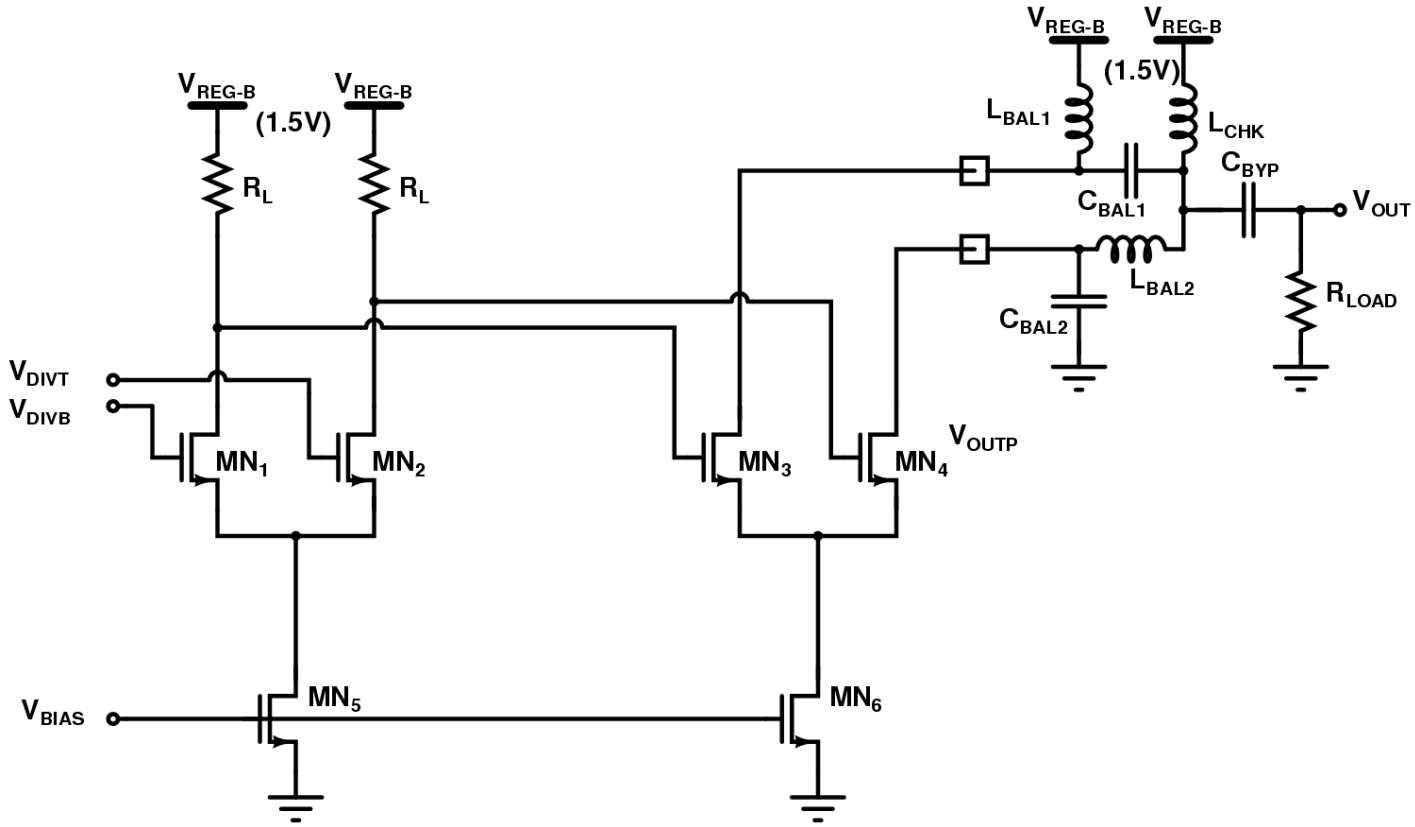
Output Buffer



DC-coupled 2-stage output buffer with external narrowband LC-based differential to single-ended combiner

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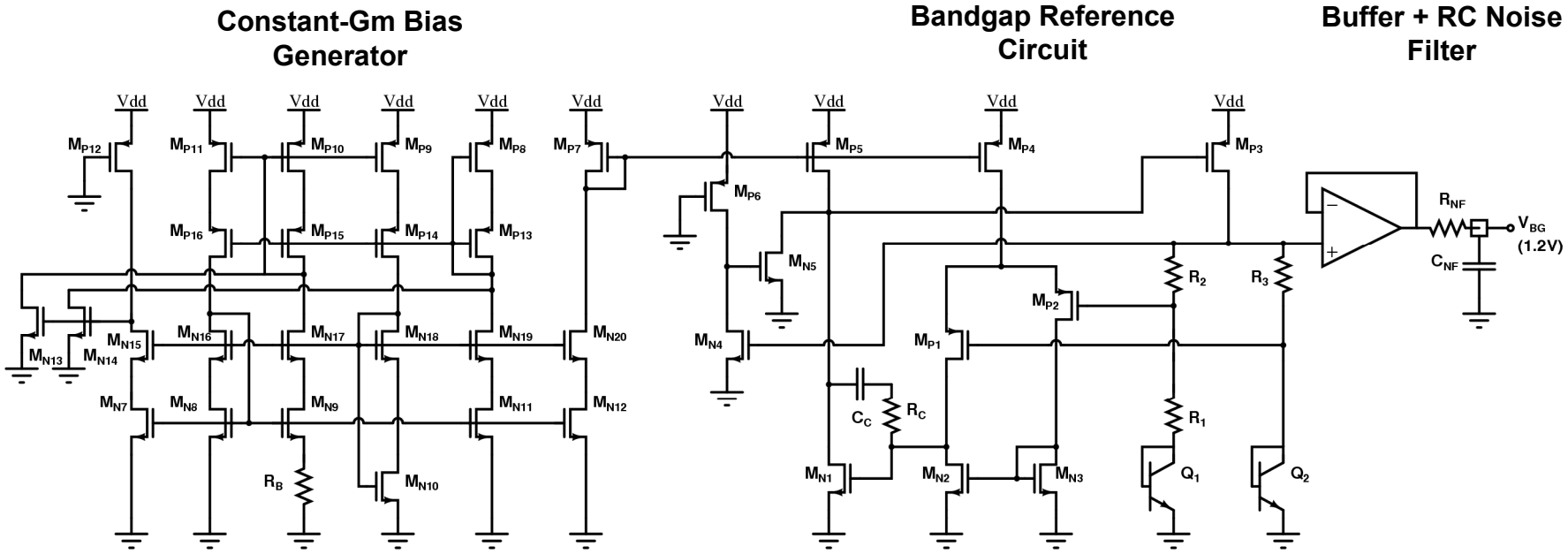
Bandgap Reference



Bandgap voltage reference with noise filter to reduce bias noise impact on VCO phase noise

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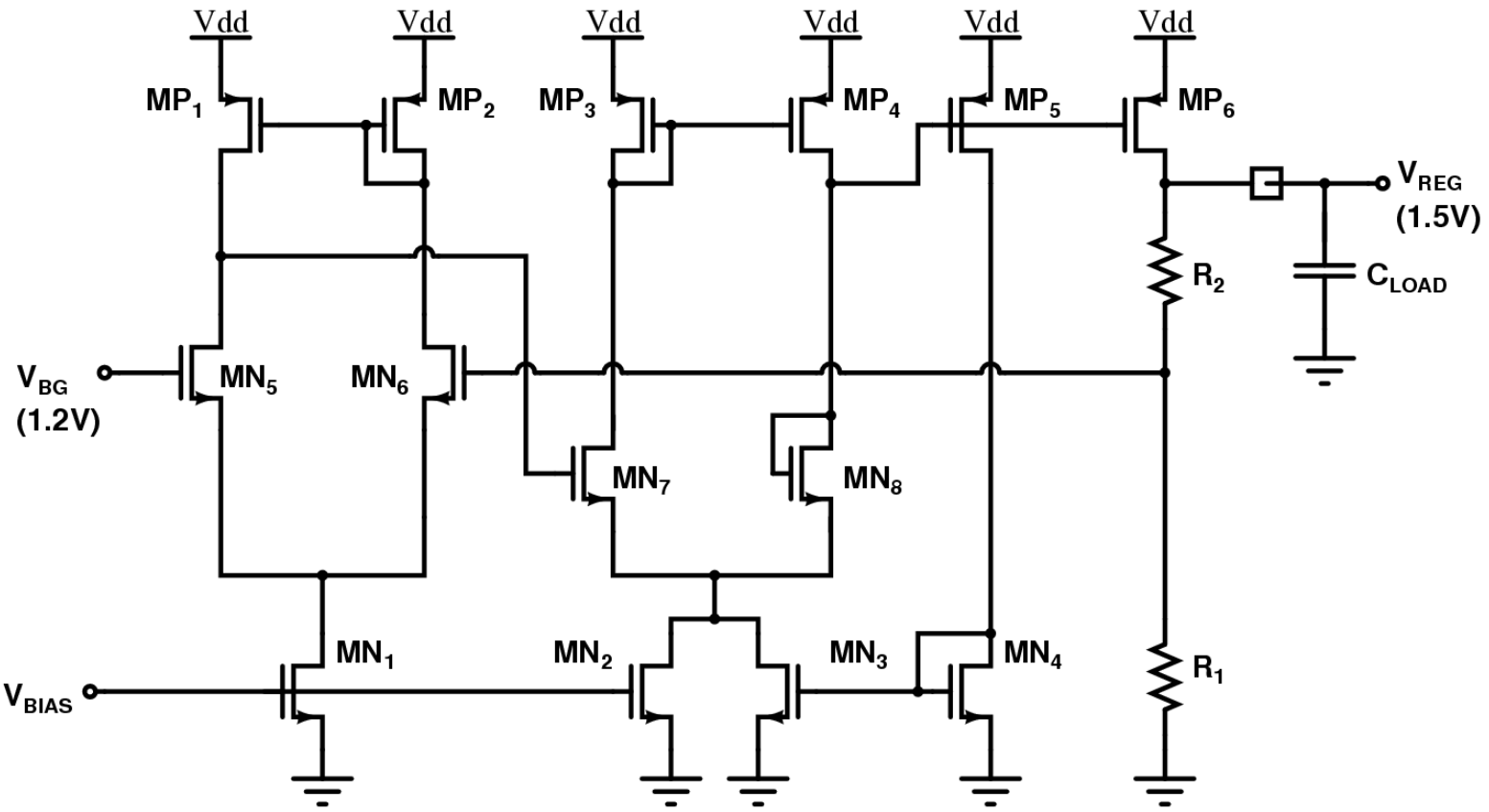
Voltage Regulator



Voltage regulator using external capacitor for good high-frequency PSRR

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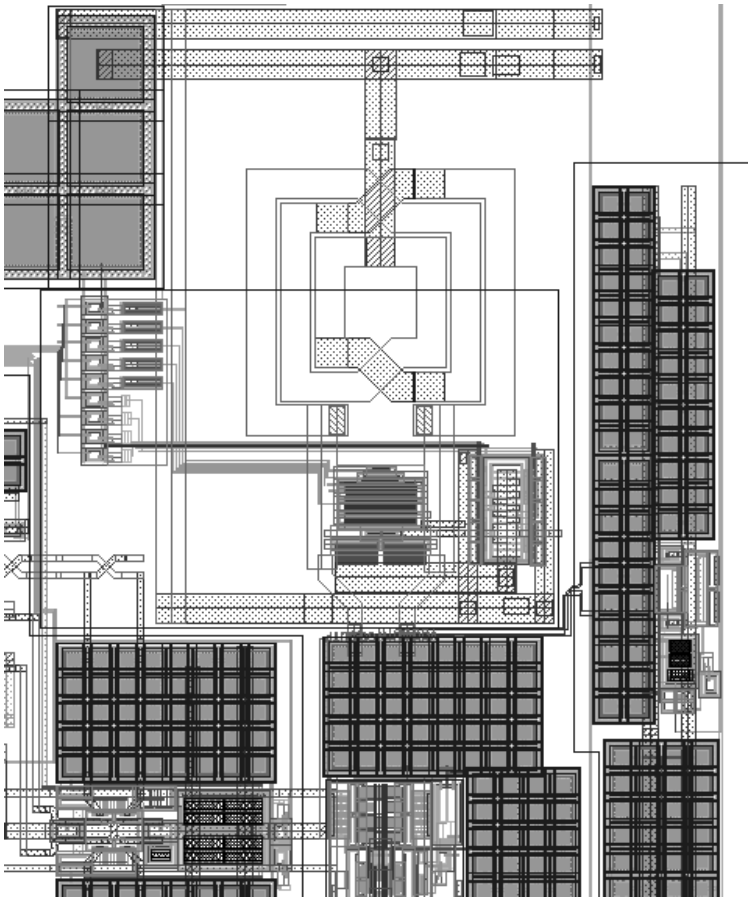
VCO Layout



Chip Area = 400um x 600um

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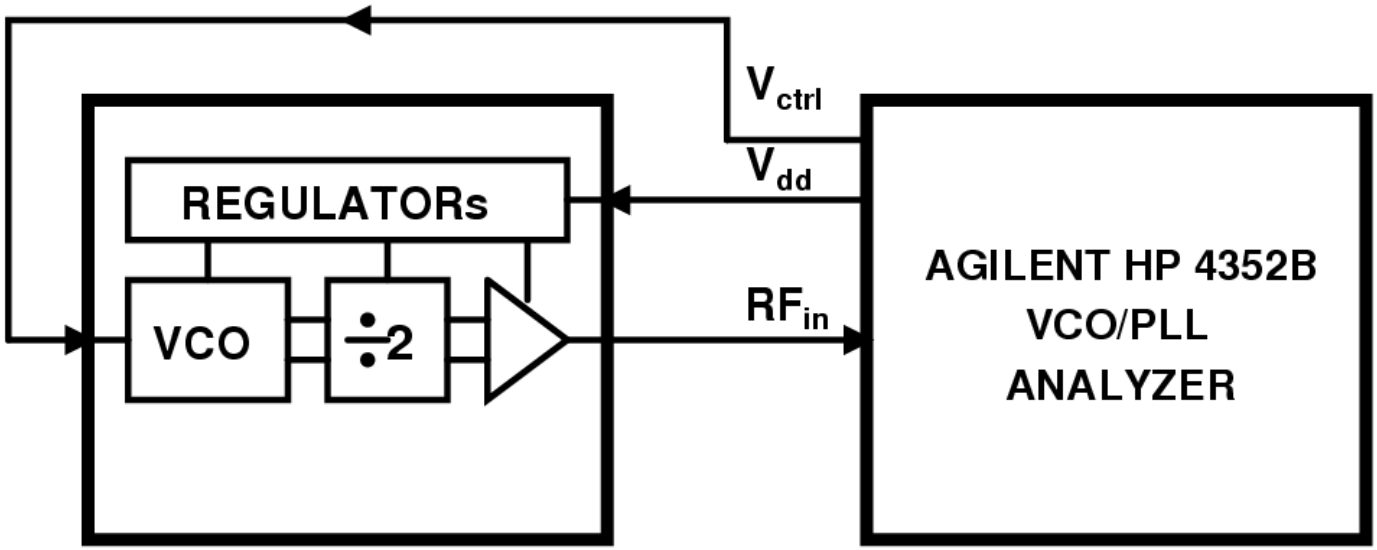
Measurement Test Setup



All VCO measurements were performed after divide-by-2 circuit

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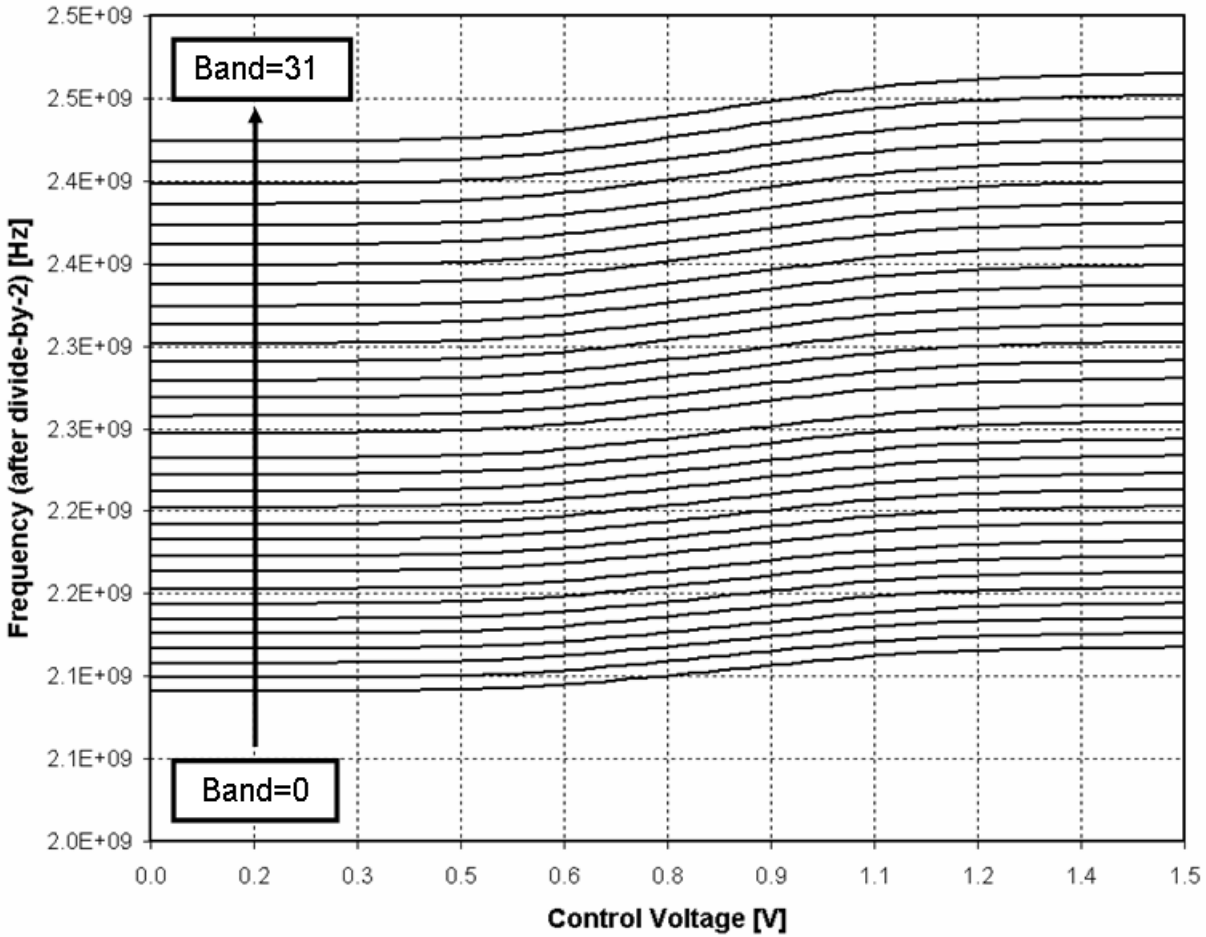
Measured Tuning (after div2)



Frequency Coverage = 2090MHz to 2470MHz

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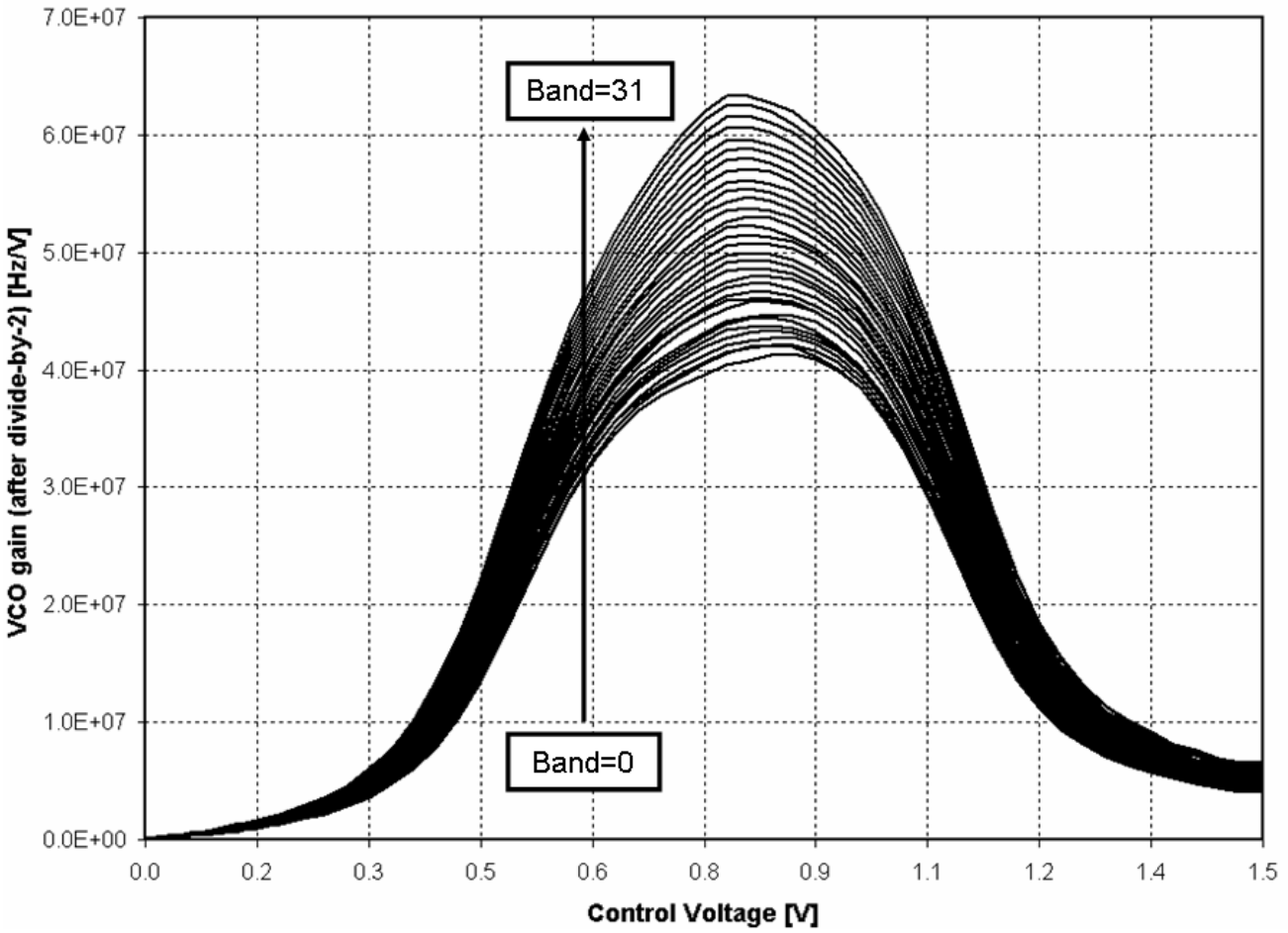
Measured VCO Gain (after div2)



VCO Gain @ 0.8V = 41MHz/V to 63MHz/V

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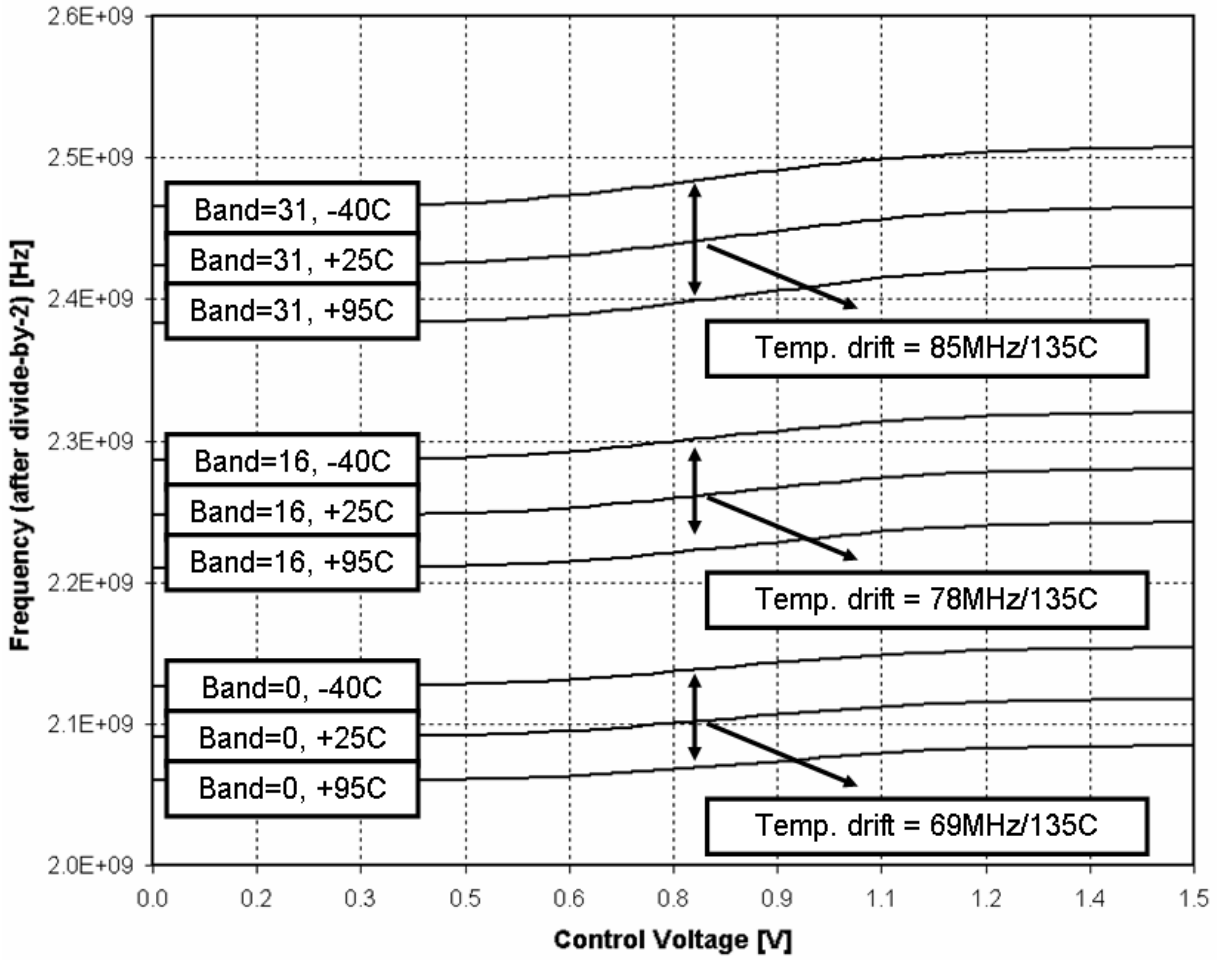
Measured Frequency Drift (after div2)



Worst case temperature drift = 85MHz/135C

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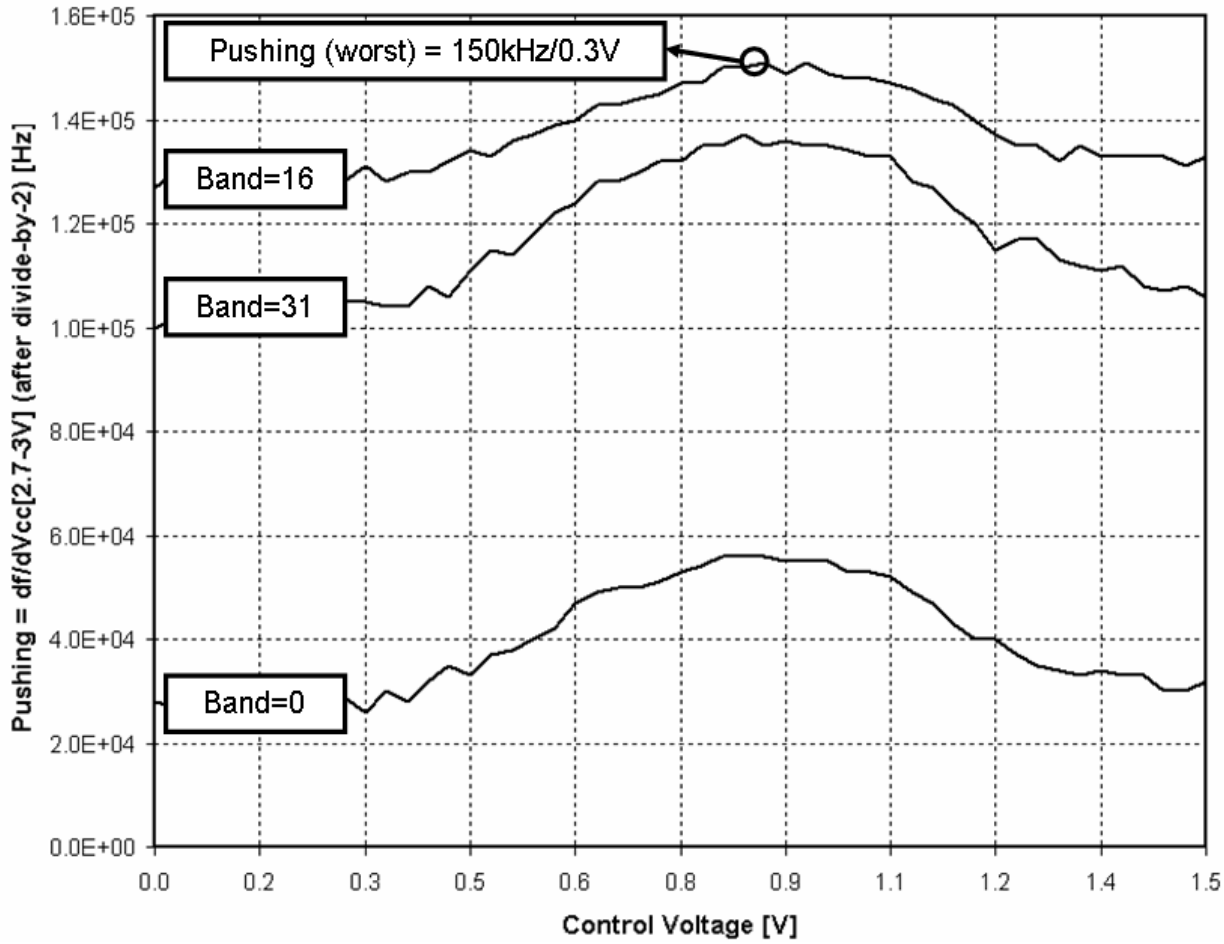
Measured Supply Pushing (after div2)



Worst Case Supply Pushing = 150kHz/0.3V

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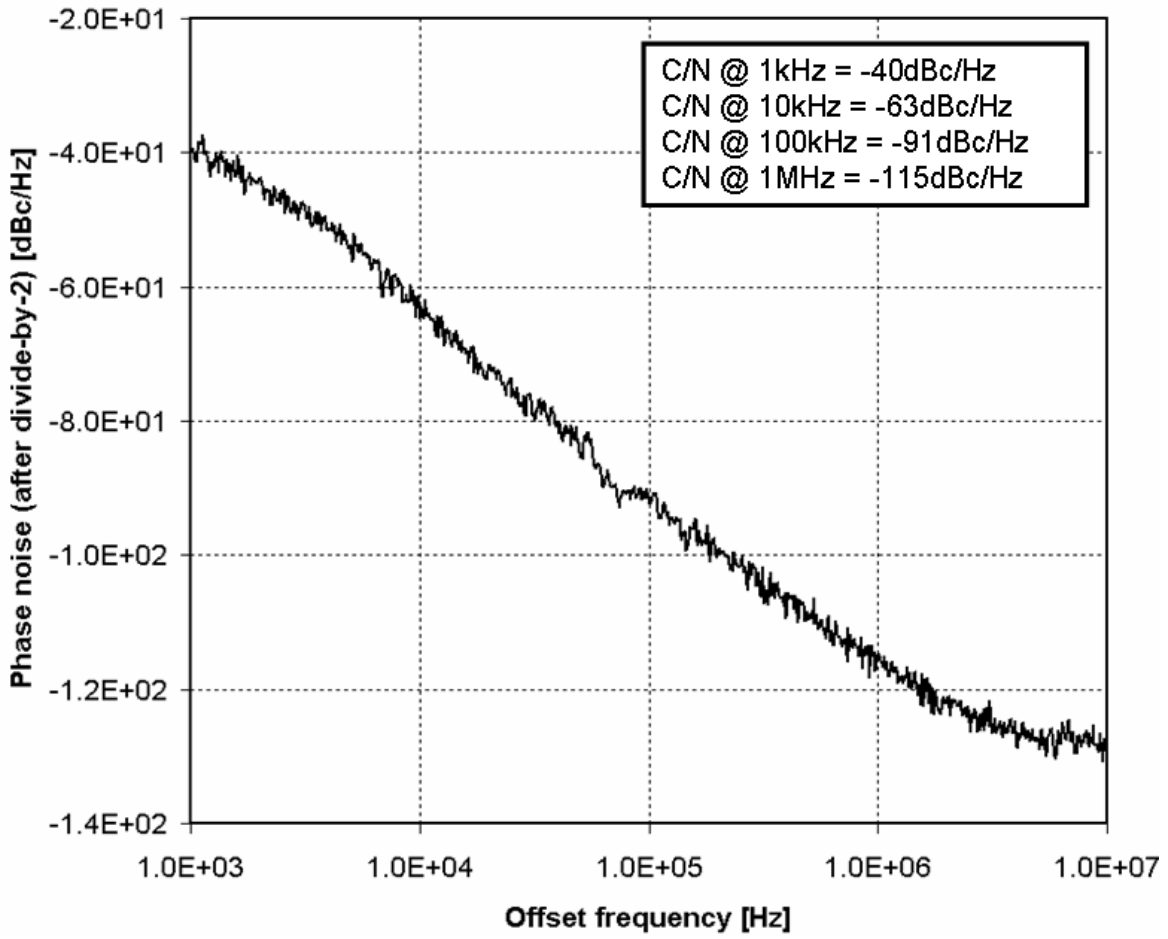
Measured Phase Noise (after div2)



Phase Noise @ 1MHz = -115dBc/Hz

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Summary

Technology	0.15um CMOS
Supply Voltage	2.7V - 3.3V
Current Consumption (VCO)	4mA
Frequency Coverage (VCO)	4180MHz – 4940MHz
VCO Gain @ 0.8V (VCO)	82MHz/V - 126MHz/V
Phase Noise @1MHz (VCO)	-109dBc/Hz
Supply Pushing (VCO) [Vcc=2.7-3.0V]	100kHz/0.1V

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Conclusion

- A technique for extending the linear range of VCO tuning transfer characteristics was demonstrated in purely digital CMOS process.

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Acknowledgements

- The authors would like to thank Prachee Behera, a former colleague.

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