

A Wide Tuning 1.3 GHz LC VCO with Fast Settling Noise Filtering Voltage Regulator in 0.18 μm CMOS Process

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Abstract — This paper presents a wide tuning LC voltage controlled oscillator (VCO) with integrated voltage regulator to minimize supply pushing. The integrated voltage regulator utilizes on-chip low-corner frequency noise filters to minimize the impact of regulator noise on VCO phase noise. One shot circuit is used with low-corner frequency noise filter to ensure fast settling. The VCO achieves current consumption of 15.9 mA with single integrated low-Q LC tank, tuning range of 620.8 MHz to 1384.5 MHz, phase noise of -128 dBc/Hz at 1 MHz offset from 1.3 GHz carrier at room temperature. With the noise filter, 9 dB improvement in phase noise is demonstrated in measurement. The frequency range can be extended to 38.8 MHz - 1384.5 MHz with integrated frequency dividers.

Index Terms — voltage regulator, voltage controlled oscillator, wide tuning range.

I. INTRODUCTION

Phase noise of local oscillators is a crucial design parameter in RF systems. For example, a transmitted signal with substantial phase noise may corrupt adjacent channel or it may lead to increased bit error rates in digital communication systems [1]. LC VCOs, instead of ring oscillators, are often used in RF transceivers for their superior phase noise characteristics [2][3]. In addition to phase noise, supply pushing can be sensitive to frequency modulation of any noise or interference present on the voltage supply of the VCO. To minimize the supply pushing, today's VCOs often use voltage regulators [4][5][6]. Although voltage regulator is helpful for reducing VCO supply pushing, its low-frequency noise can be modulated with the VCO frequency and negatively impact its phase noise. A common technique to reduce regulator noise is to use large off-chip noise-filtering capacitors. Although this technique is very effective at reducing regulator noise, in applications where chip pin count is important, it may be desirable to use a regulator which does not require any external pins.

This paper presents a noise filtering technique with fast settling time for a voltage regulator, which offers a small layout area, no external components, and sufficient noise suppression, implemented in a 1.3 GHz wideband LC VCO design. The implemented prototype also integrates frequency dividers and buffers.

II. PROPOSED TECHNIQUE

Figure 1 (a) shows a conventional method of implementing a low noise and high power supply rejection voltage regulator [7][8]. The bandgap voltage reference ensures constant voltage over supply and temperature variations, and voltage regulating amplifier scales up the 1.2 V bandgap voltage to desired regulated voltage by the ratio of resistors R2 and R1. External capacitors, C2 and C3, help achieving low noise and good power supply rejection.

Figure 1 (b) shows the proposed approach. To implement low-corner frequencies (<1kHz) needed to filter out regulator noise, noise filters using moderate-size on-chip capacitors and long channel MOS transistors are proposed. In addition, to minimize the noise impact of the bandgap voltage scaling amplifier noise, the VCO supply voltage is regulated using a unity gain regulator. Although it's possible to regulate the VCO directly using bandgap voltage scaling amplifier, the proposed architecture achieves better regulator noise. Since these noise filters have low-frequency cut-offs, the proposed regulator is very slow to settle. To realize fast settling time, one shot circuit is used to momentarily bypass the long-channel triode resistors and quickly pre-charge filtering capacitors to their steady-state voltages. After one shot signal turns OFF, the noise filters are enabled, and the regulator operates at its normal low noise mode.

III. CIRCUIT DESIGN

A. Architecture

The LC VCO is designed to oscillate from 650 MHz to 1300 MHz. A tuning range of 2:1 is chosen so that frequency dividers can be used to extend the tuning range down to 650MHz/16.

The two buffers are connected to the VCO output in order to impose equal loading to the VCO. This is done to minimize VCO frequency pulling when stepping through different divider modes. Frequency dividers are implemented with conventional CML divider circuits [9].

B. Bandgap Reference Design

Bandgap voltage reference circuit used in this design is shown in Figure 3. The bandgap core consists of transistors Q1 and Q2 and resistors R1, R2, and R3. The error amplifier formed by M1, M2, M3, and M4 and the output transistor M5 creates negative feedback needed to regulate the bandgap. A long channel transistor M10 and Miller capacitor C1 form a noise filter to minimize bandgap noise. This noise filter is also bypassed using one shot circuit to speed-up bandgap voltage itself via M6 and R4. A start-up circuit is used to ensure proper bandgap start-up. Diodes D1 and D2 are used to short the long-channel MOS in case of large unexpected transition to speed up recovery time.

C. VCO Design

A wide tuning LC VCO is designed to demonstrate the effectiveness of the noise filtering voltage regulator on the VCO phase noise performance. The schematic of the VCO is shown in Figure 4. The wideband LC VCO is implemented in a complementary cross-coupled differential topology to achieve low phase noise with high power efficiency. To minimize VCO phase noise, low VCO gain is chosen [10]. To provide large frequency coverage, 7-bit binary-weighted MIM capacitor array is used. The complementary cross-coupled pair consists with seven switchable pair and one fixed pair. The seven switchable pairs are sized in binary-weighted fashion and track with the 7-bit MIM capacitor coarse tuning for high power efficiency. The number of turned ON pair decreases as the number of MIM capacitor array decreases because the quality factor looking into the MIM capacitor array increases in this case. A 3-bit programmable resistor array is used for post fabrication current and phase noise optimization. Accumulation varactors are used for the fine frequency tuning and implemented in differential fashion to maximize the quality factor [11]. Only one integrated inductor is used.

IV. MEASUREMENT RESULTS

The noise filtering voltage regulator, wideband VCO, divider, and buffer circuits were fabricated in a 0.18 μm CMOS process. Figure 5 shows the chip layout. The chip has been packaged in QFN24 package and was mounted on a conventional FR4 device evaluation board. All measurements were done using Agilent 5052B Signal Source Analyzer.

Figure 6 shows the measured tuning characteristic for all 128 bands. The measured tuning range is from 620.5 MHz to 1384.5 MHz for bands 0 to 127, respectively. The

tuning range can be extended to from 38.8 MHz to 1384.5 MHz using the four divide-by-two circuits.

The peak VCO gain varies from 4.2 MHz/V to 41.4 MHz/V for band 0 to 127, respectively. The low VCO gain at low band setting is caused by the cross-coupled CMOS pair parasitic, which constitutes a significant portion of the tank capacitance [12]. The switchable cross-coupled CMOS pair parasitic contribution increases as the coarse tuning band decreases as well as the MIM capacitor contribution increases.

Figure 8 shows the measured phase noise when the noise filtering is turned ON and OFF, and the control voltage was fixed at 1.4 V. The phase noise is -102 dBc/Hz at 100 kHz offset and -128 dBc/Hz at 1 MHz offset from 1.3 GHz carrier with the noise filtering is turned ON. On the other hand, the phase noise where the noise filtering is turned OFF is -93 dBc/Hz at 100 kHz offset and -119 dBc/Hz at 1 MHz offset from the carrier. The measured data shows an improvement of 9 dB in VCO phase noise at 1 MHz offset from 1.3 GHz carrier.

Figure 9 shows the measured temperature drift of the VCO. The measured temperature drift is 14 MHz/115C, 15 MHz/115C, and 13 MHz/115C for bands 0, 63, and 127, respectively. The temperature drift is larger than the frequency tuning coverage at lower bands. Although for TDMA type application this may not be a problem since the synthesizer is periodically re-locked, it is a critical problem for CDMA type applications where synthesizer must stay locked over entire temperature range and cannot be re-locked. To reduced temperature drift, temperature compensation circuit is necessary [13][14].

The measured supply pushing is less than 0.5 MHz/0.3V for band 0 and 63. However, at band 127 supply pushing is 1.5 MHz/0.3V, which is higher than expected.

The VCO current consumption, including the regulator, varies from 9.9 mA to 15.9 mA, depending on the bands selected, from the 3.3 V supply. In order to achieve the tuning range of 2:1, the relatively high current consumption was necessary to compensate for the low Q-factor of the single integrated inductor ($Q=8$) whereas typical external inductors have Q-factor as high as 40.

V. CONCLUSION

A wide tuning LC VCO with integrated voltage regulator, which uses on-chip noise filters to achieve low noise and one shot circuit to achieve fast settling, has been demonstrated in 0.18 μm CMOS process. The effectiveness of the proposed regulator has been confirmed by measurements where 9 dB of improvement in phase noise at 1 MHz offset from carrier of 1.3 GHz

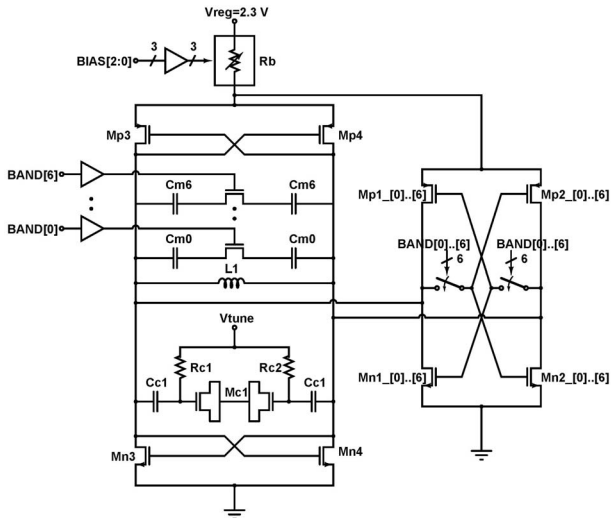


Fig. 4. Schematic of the wideband LC VCO.

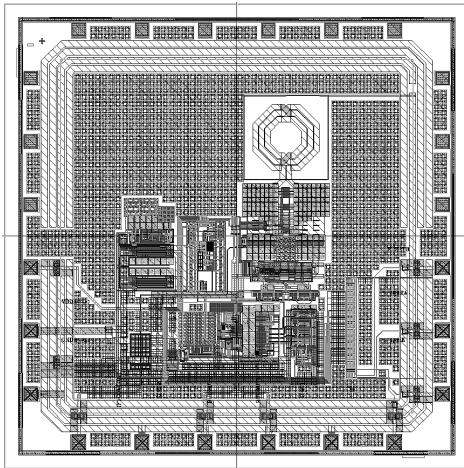


Fig. 5. Layout diagram of the wideband LC VCO chip.

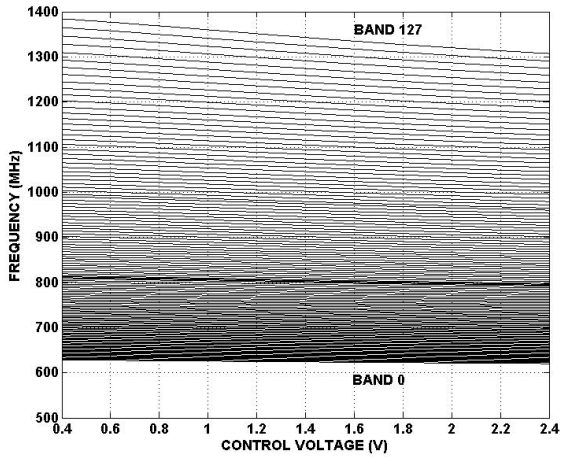


Fig. 7. Measured frequency tuning.

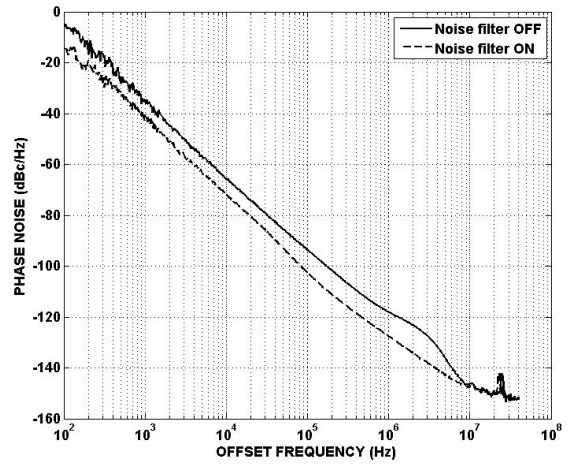


Fig. 8. Measured phase noise (1.3 GHz carrier).

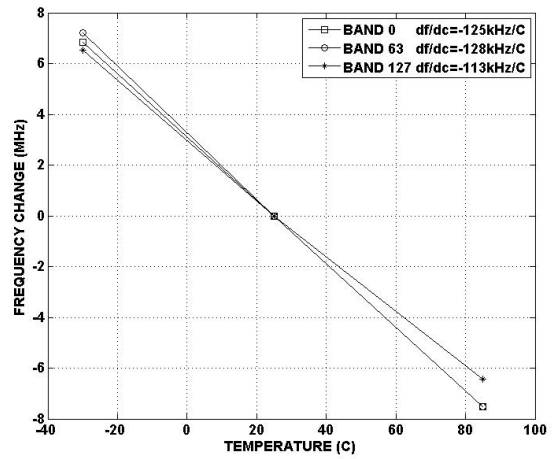


Fig. 9. Measured temperature drift.

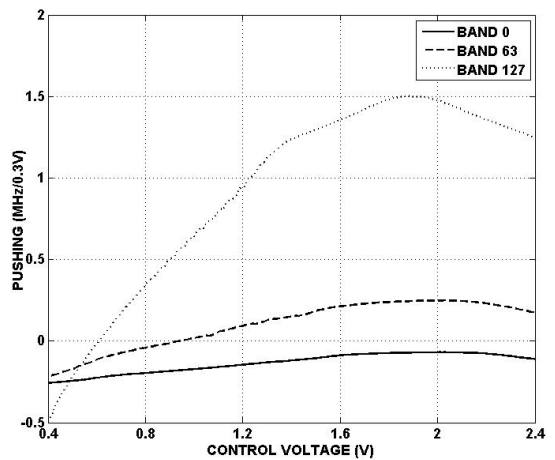


Fig. 10. Measured supply pushing.