50Msps 12-Bit SAR ADC IP Marketing Brief

Epoch Microelectronics, Inc.

Valhalla, NY

12-Bit 50Msps SAR ADC: Features/Deliverables

Features:

- Non-binary switch capacitor SAR ADC architecture that relaxes voltage reference settling requirements
- Incorporates calibration logic to calibrate linearity of SAR ADC
- Includes delay lock loop for internal high speed clock generation

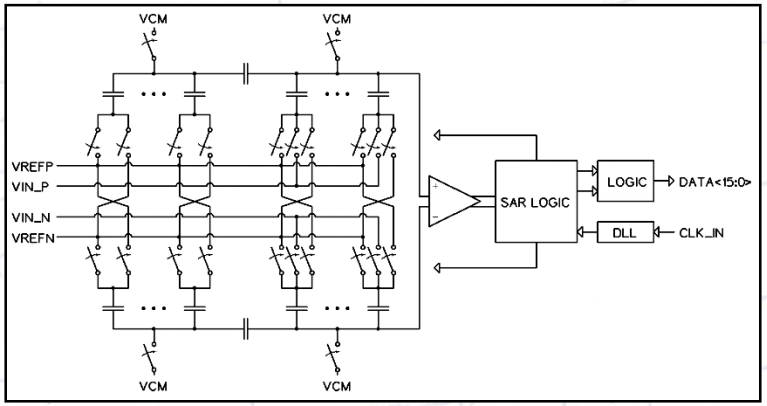
Deliverables:

- White Box:
  - Cadence library including schematics, layout, and test benches
  - GDS2, CDL netlist, DRC/LVS/ERC reports
  - Verilog and .LIB files
  - Evaluation report
- Black Box:
  - GDS2, CDL netlist, DRC/LVS/ERC reports
  - Verilog and .LIB files
  - Encrypted SPICE netlist
  - Evaluation report

epoch microelectronics

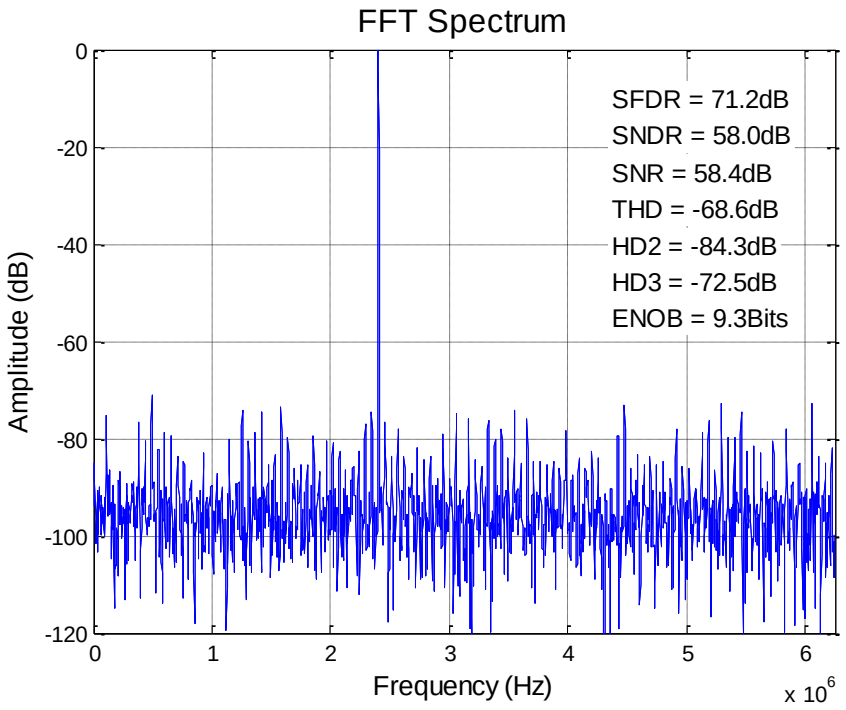
12-Bit 50Msps Switch Capacitor SAR ADC

Technology	Global Foundries 40nm CMOS
Process Options	6L1x_1T6x_1T18x_LB
Analog Supply Voltage	1.1V/1.8V
Digital Supply Voltage	1.1V
Sampling Rate	50Msps
Input Voltage Swing	$2.2V_{ppd}$
ENOB	9.4bit (10.2 @40Msps)
SNDR	58.1dB (63dB @40Msps)
Active Chip Area	$0.15mm^2$
Power (Analog)	4.1mW
Power (Digital)	6.1mW
Status	*Respin needed – See Errata Slide*

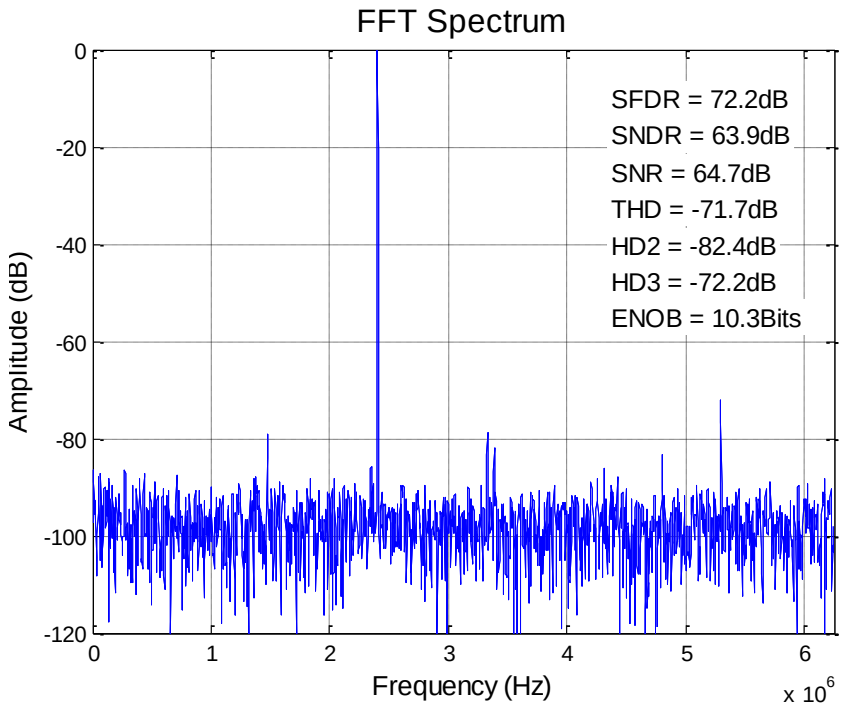


Measured Spectrum: TT Sample @ 12.5Msps

Uncalibrated ADC



Calibrated/adjusted ADC



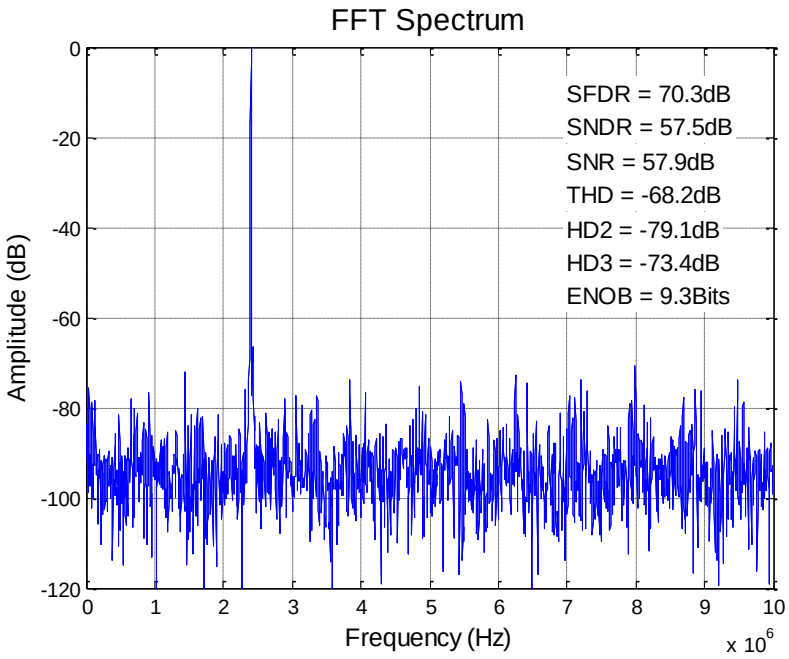
ENOB = 9.3 (uncalibrated) / 10.3 (calibrated)

Measurement Conditions: Vin = 2.2Vppd, Fs = 12.5Msps, Temp = Room, ADC Calibration = Disabled

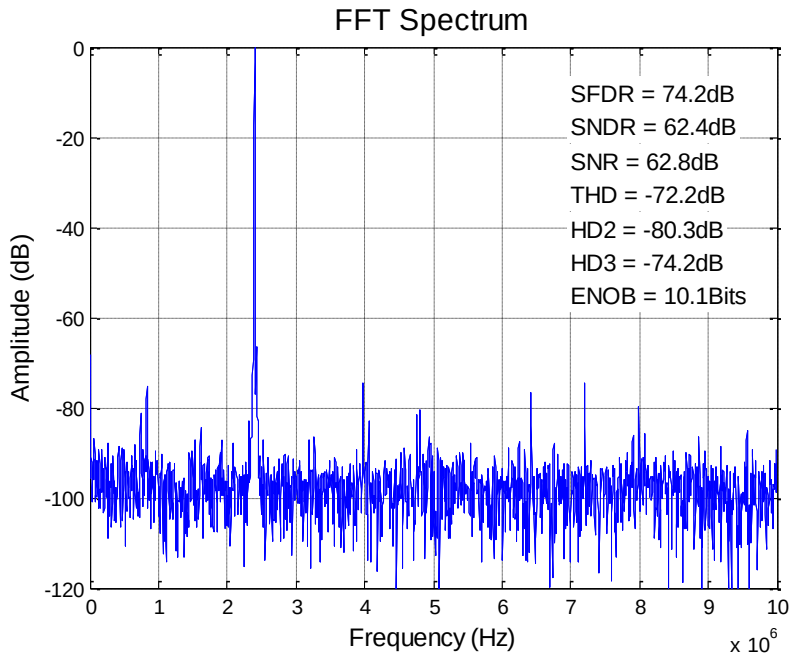
epoch microelectronics

Measured Spectrum: TT Sample @ 20Msps

Uncalibrated ADC



Calibrated/adjusted ADC



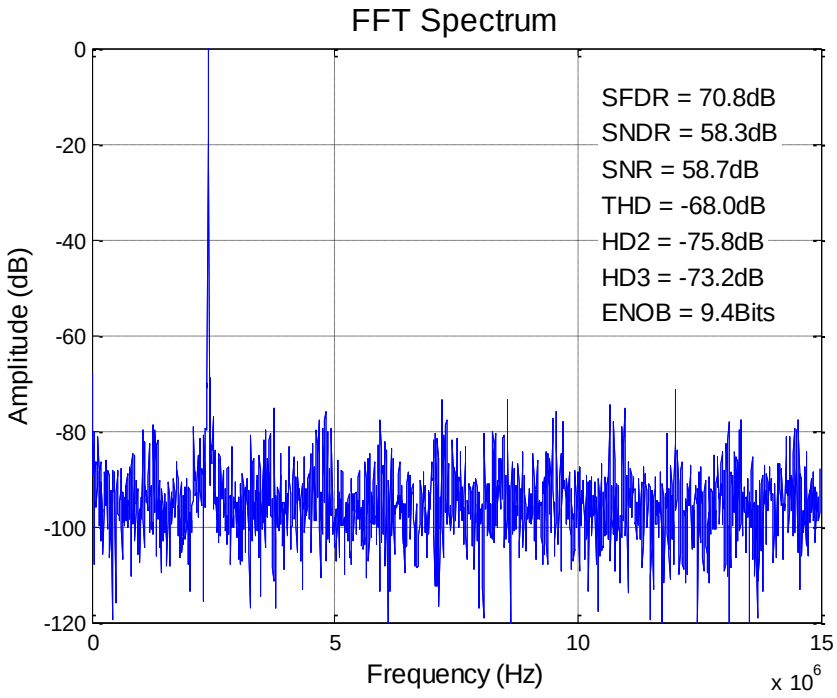
ENOB = 9.3 (uncalibrated) / 10.1 (calibrated)

Measurement Conditions: Vin = 2.2Vppd, Fs = 20Msps, Temp = Room, ADC Calibration = Disabled

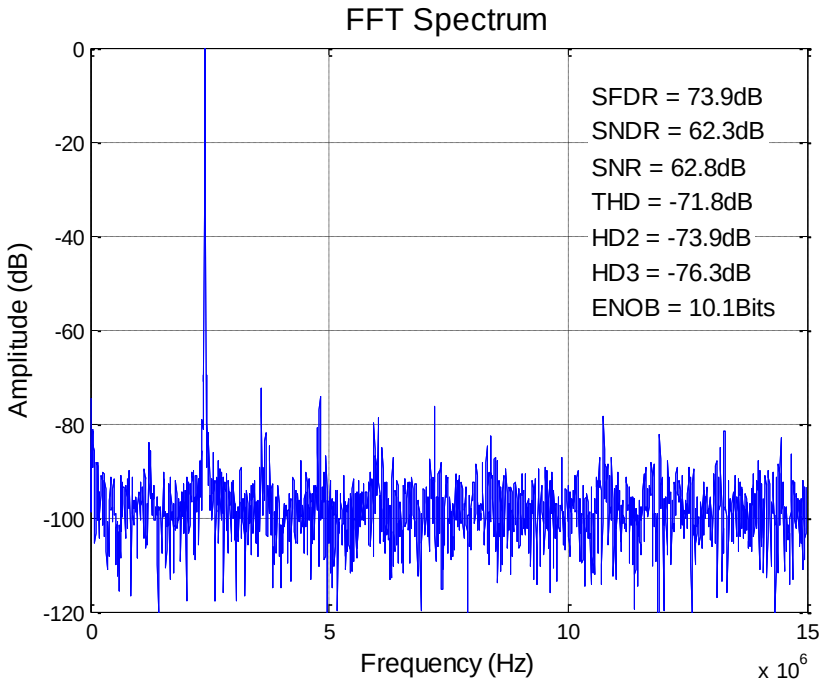
epoch microelectronics

Measured Spectrum: TT Sample @ 30Msps

Uncalibrated ADC



Calibrated/adjusted ADC



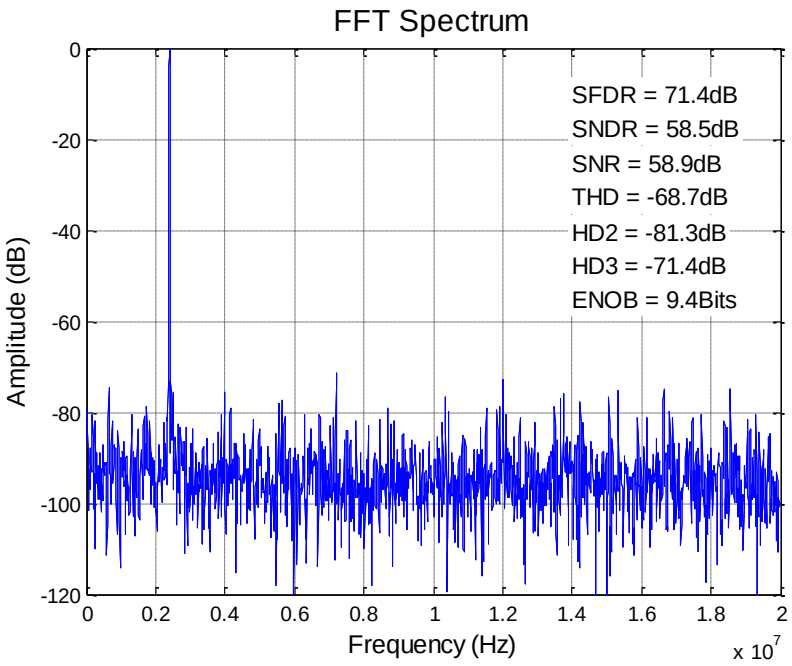
ENOB = 9.4 (uncalibrated) / 10.1 (calibrated)

Measurement Conditions: Vin = 2.2Vppd, Fs = 30Msps, Temp = Room, ADC Calibration = Disabled

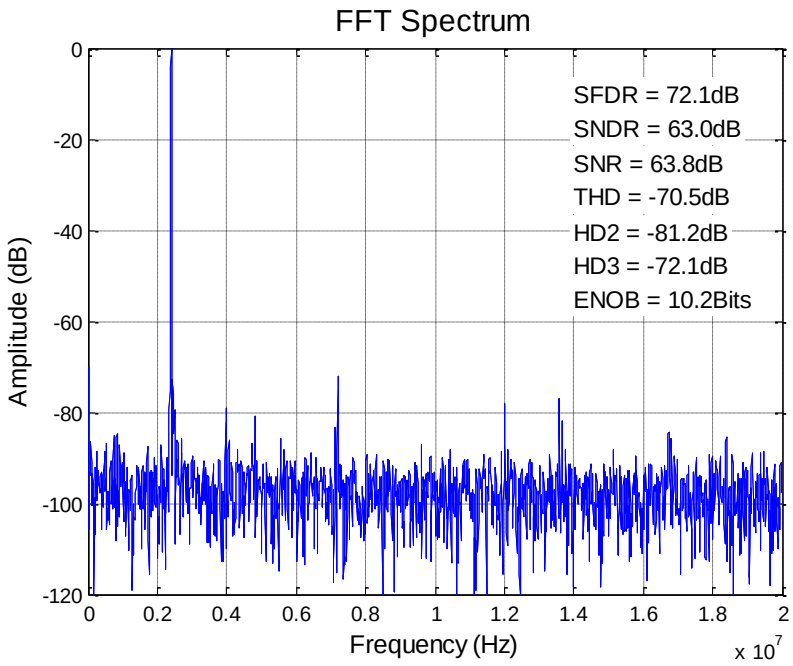
epoch microelectronics

Measured Spectrum: TT Sample @ 40Msps

Uncalibrated ADC



Calibrated/adjusted ADC



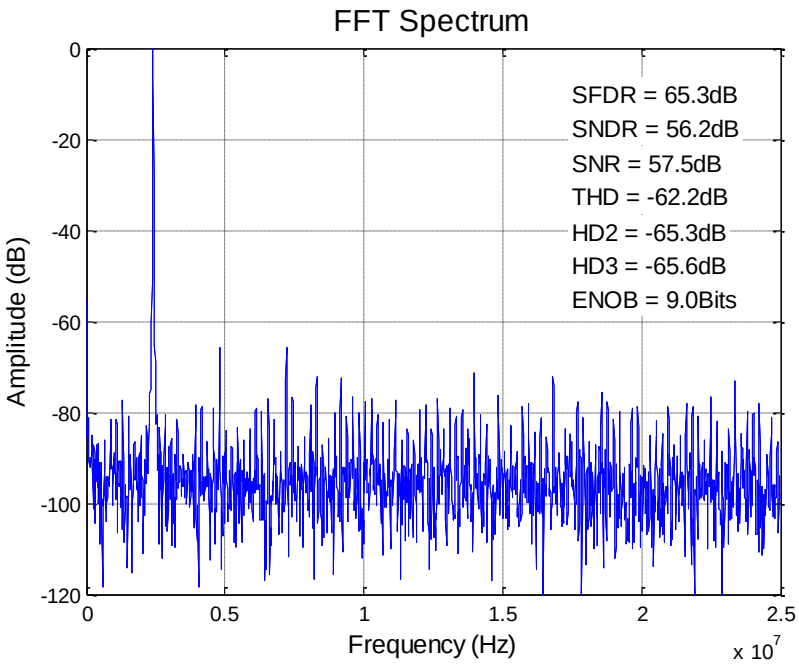
ENOB = 9.4 (uncalibrated) / 10.2 (calibrated)

Measurement Conditions: Vin = 2.2Vppd, Fs = 40Msps, Temp = Room, ADC Calibration = Disabled

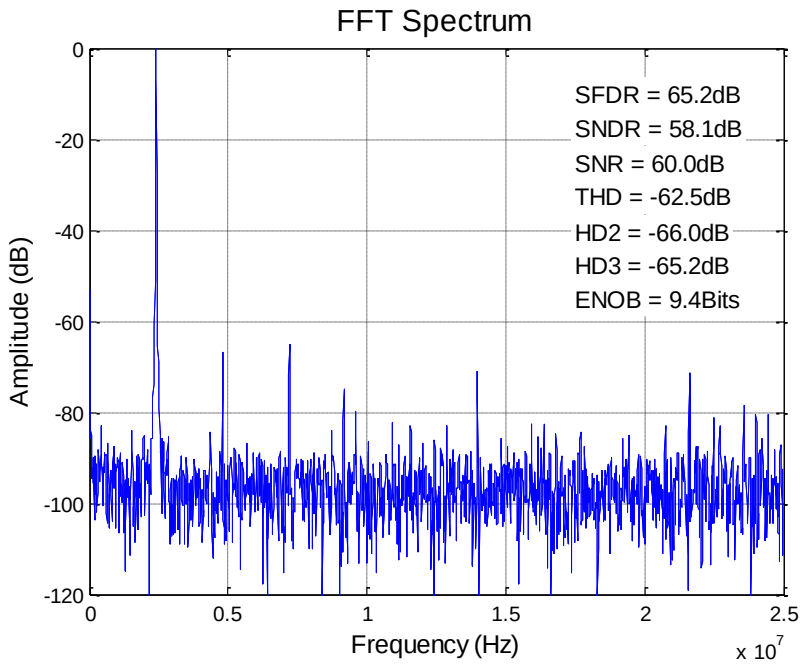
epoch microelectronics

Measured Spectrum: TT Sample @ 50Msps

Uncalibrated ADC



Calibrated/adjusted ADC



ENOB = 9.0 (uncalibrated) / 9.4 (calibrated)

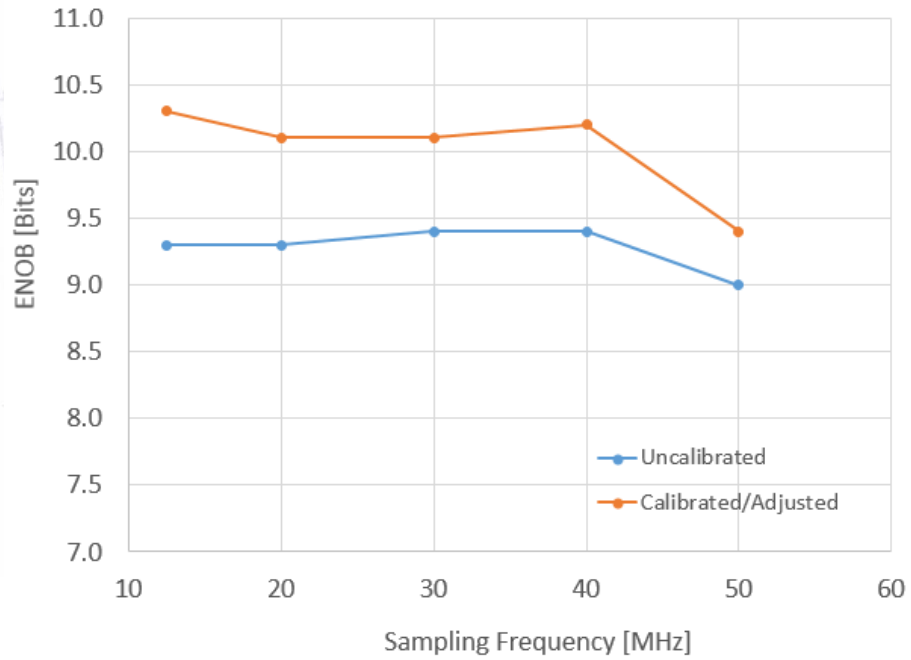
Measurement Conditions: Vin = 2.2Vppd, Fs = 50Msps, Temp = Room, ADC Calibration = Disabled

epoch microelectronics

Measured ENOB vs Sampling Frequency

Fsample (MHz)	12.5	20	30	40	50
Uncalibrated	9.3	9.3	9.4	9.4	9.0
Calibrated/Adjusted	10.3	10.1	10.1	10.2	9.4

[Unit: Bits]



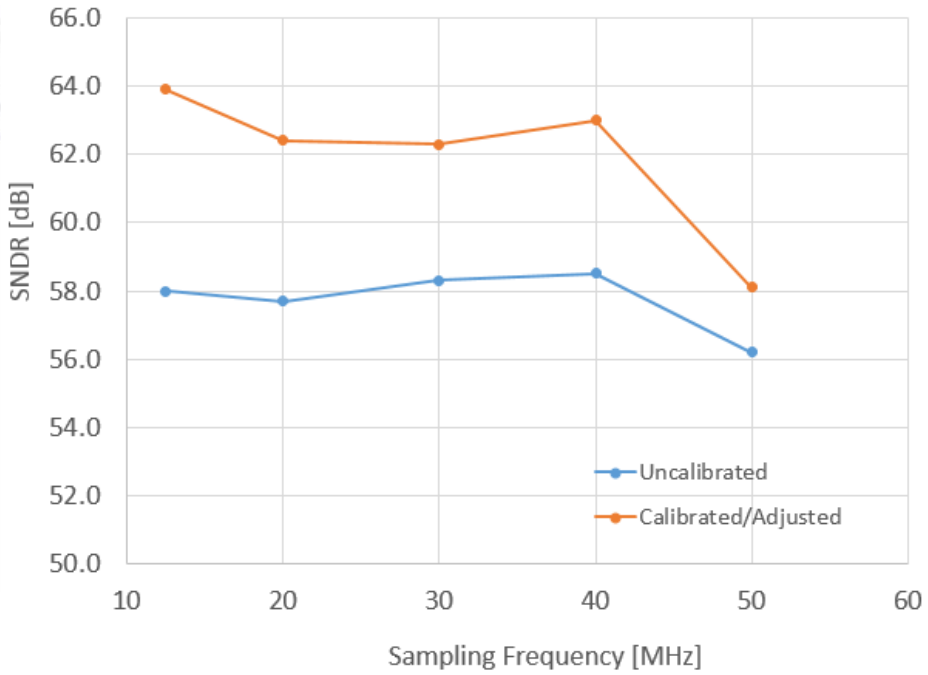
Measurement shows degradation at 50Msps

epoch microelectronics

Measured SNDR vs Sampling Frequency

Fsample (MHz)	12.5	20	30	40	50
Uncalibrated	58.0	57.7	58.3	58.5	56.2
Calibrated/Adjusted	63.9	62.4	62.3	63.0	58.1

[Unit: dB]



Measurement shows degradation at 50Msps

epoch microelectronics

Errata

(1) ADC calibration logic does not have enough range (i.e. bit length) and MSB correction value saturates to maximum code. Verilog needs to be updated and synthesis/P&R must be repeated to fix this issue.

(2) DLL DCO reset pulse is too long which results at shorter sampling/conversion cycles not allowing time to settle at 50Msps

Thank you!

Ken Suyama
Email: ken.suyama@epochmicro.com
Phone: 914-332-8570x222